Vertical GaN and SiC Power Devices

Kazuhiro Mochizuki

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Preface

Compared with silicon, both gallium nitride (GaN) and silicon carbide (SiC) have excellent physical properties; the electric field that results in breakdown is more than 10 times higher, and the thermal conductivity is 33%–330% higher. They are therefore expected to be the ultimate materials for power devices used in highly efficient power-electronics systems. In the case of GaN, recent progress concerning high-quality freestanding substrates has dramatically improved the performance of vertical power devices. However, in the latest book on GaN and SiC power devices, this improved performance is only mentioned briefly in a 10-page-long chapter [1]. In view of that situation, this book is intended to provide a comparative introduction to vertical GaN and SiC power devices for students, researchers, and engineers working in the field of crystal growth, processing, and design for power semiconductor devices.

I started writing this book after receiving an offer from Artech House following a talk I was invited to give entitled "Vertical GaN Bipolar Devices: Gaining Competitive Advantage from Photon Recycling" at the International Symposium on Compound Semiconductors in 2016 [2]. The emphasis in this book is therefore partly on photon recycling (Chapter 4), which is important for increasing not only the effective minority-carrier lifetime but also the ionization ratio of deep acceptors. Photon recycling in GaN is attributable to very large peripheral current flowing through non-self-aligned mesa-type p-n junctions (Chapter 3). This phenomenon has not been described in any books, since forward current flowing through p-n junctions has been treated one-dimensionally only.

In addition, to the best of my knowledge, all the books on GaN and SiC power devices inadequately describe Schottky junctions; namely, they describe thermionic emission as a limiting process on current transport even though electron mobility becomes quite low under a high electric field. As described in Chapter 8, diffusion is more important, especially when electron mobility is reduced by ion-implantation-induced damage or phonon scattering at elevated temperatures.

Among unipolar power-switching devices, SiC superjunction power-switching devices are expected to have the lowest specific on-resistance around a breakdown voltage of 6.5 kV. Although trench-filling epitaxy is indispensable for fabricating Si and SiC superjunction devices, the trench-filling mechanisms in the cases of silicon and SiC are completely different. Chapter 6 is thus dedicated to explaining such epitaxial growth mechanisms.

Other topics that have not been covered in previous books on power semiconductor devices include the following: a comparison of vertical and lateral power-semiconductor devices based on reported results (Chapter 1), modeling of aluminum and boron profiles in SiC (Chapter 7), GaN bipolar junction transistors (Chapter 10), and a comparison of junction terminations and reliability of vertical GaN and SiC power devices (Chapters 11 and 12).

I wrote this book with the help of valuable supporting discussions with professor Tomoyoshi Mishima of Hosei University on extrinsic photon recycling (Chapter 4); Professor Emeritus Tatau Nishinaga of the University of Tokyo on supersaturation of spiral growth and the Gibbs–Thomson effect (Chapter 6); professor Toshikazu Suzuki of the Japan Advanced Institute of Science and Technology on Schottky junctions (Chapter 8); and anonymous reviewers from Artech House on the whole manuscript. I also thank Dr. Yasuhiro Shimamoto, Dr. Akio Shima, and Dr. Yuki Mori of Hitachi for their support in improving the manuscript.

References

[1] Baliga, B. J., *Gallium Nitride and Silicon Carbide Power Devices,* Singapore: World Scientific, 2017, pp. 391–400.

[2] Mochizuki, K., "Vertical GaN Bipolar Devices: Gaining Competitive Advantage from Photon Recycling," *International Symposium on Compound Semiconductors*, Toyama, Japan, June 26–30, 2016, paper ThB2-1.

CHAPTER

1

Contents

1.1 Introduction

1.2 Typical Power Device Characteristics

1.3 Vertical versus Lateral Unipolar Power Devices

1.4 Summary

Vertical versus Lateral Power Semiconductor Devices

1.1 Introduction

Success of silicon-based electron devices triggered rapid progress in microelectronics and nanoelectronics that deal with relatively low power (i.e., less than 10W) (Figure 1.1). Even in power electronics dealing with much higher power, silicon-based devices have played a dominant role in recent decades; however, they are reaching the limit of progress set by fundamental material properties. Wide-bandgap semiconductors have thus attracted great attention as materials for next-generation power devices since they have superior material properties compared to silicon (see Section 2.7).

The most advanced wide-bandgap semiconductor is silicon carbide (SiC); note, for example, that its implementation into railcar-traction inverters significantly reduced power loss [1]. Another material for next-generation power

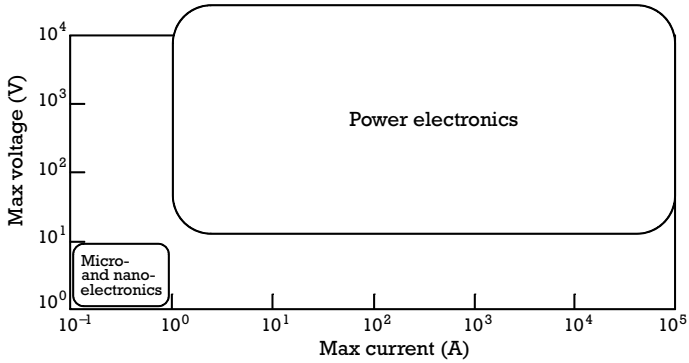

Figure 1.1 Areas of microelectronics, nanoelectronics, and power electronics as a function of maximum voltage and current.

devices is gallium nitride (GaN). Lateral power-switching devices that use GaN layers on Si substrates have a great impact on the cost-effectiveness of switching-mode power supply as well as consumer electronics [2] (see Section 1.3.1.1). Moreover, vertical GaN power devices have also attracted significant attention for their large current-handling capability [3]. As shown by the upward arrows in Figure 1.2(a, b), both SiC and GaN are expected to increase current rating (by increasing current density in the chip) and operating frequency, as described in Section 2.7. This chapter compares vertical and lateral GaN and SiC power devices in Section 1. 3.

1.2 Typical Power Device Characteristics

Power semiconductor devices are used as both switches and diodes [4] in power electronics, where electrical energy is converted from AC to DC (rectifier), DC to DC (DC-to-DC converter), and DC to AC (inverter). A diode is a two-terminal device that allows current to pass in one direction (from anode to cathode) while blocking current in the opposite direction (up to breakdown voltage [*BV*] shown in Figure 1.3). As shown in Figure 1.4, a typical three-phase voltage-source inverter, which outputs an AC voltage to a three-phase balanced load [5], uses six switches and six diodes. When the loads are inductive (e.g., in the case of motors), the diodes are used as reverse conducting devices (because most semiconductor switches conduct current in a single direction only).

While the forward-current and voltage characteristics of a power-semiconductor diode show an offset voltage (Figure 1.3), a power-semiconductor switching device has either zero-offset-voltage characteristics (Figure 1.5[a]) or offset-voltage characteristics (Figure 1.5[b]); in both cases, it exhibits forward voltage drop V_F when it carries forward current I_F.

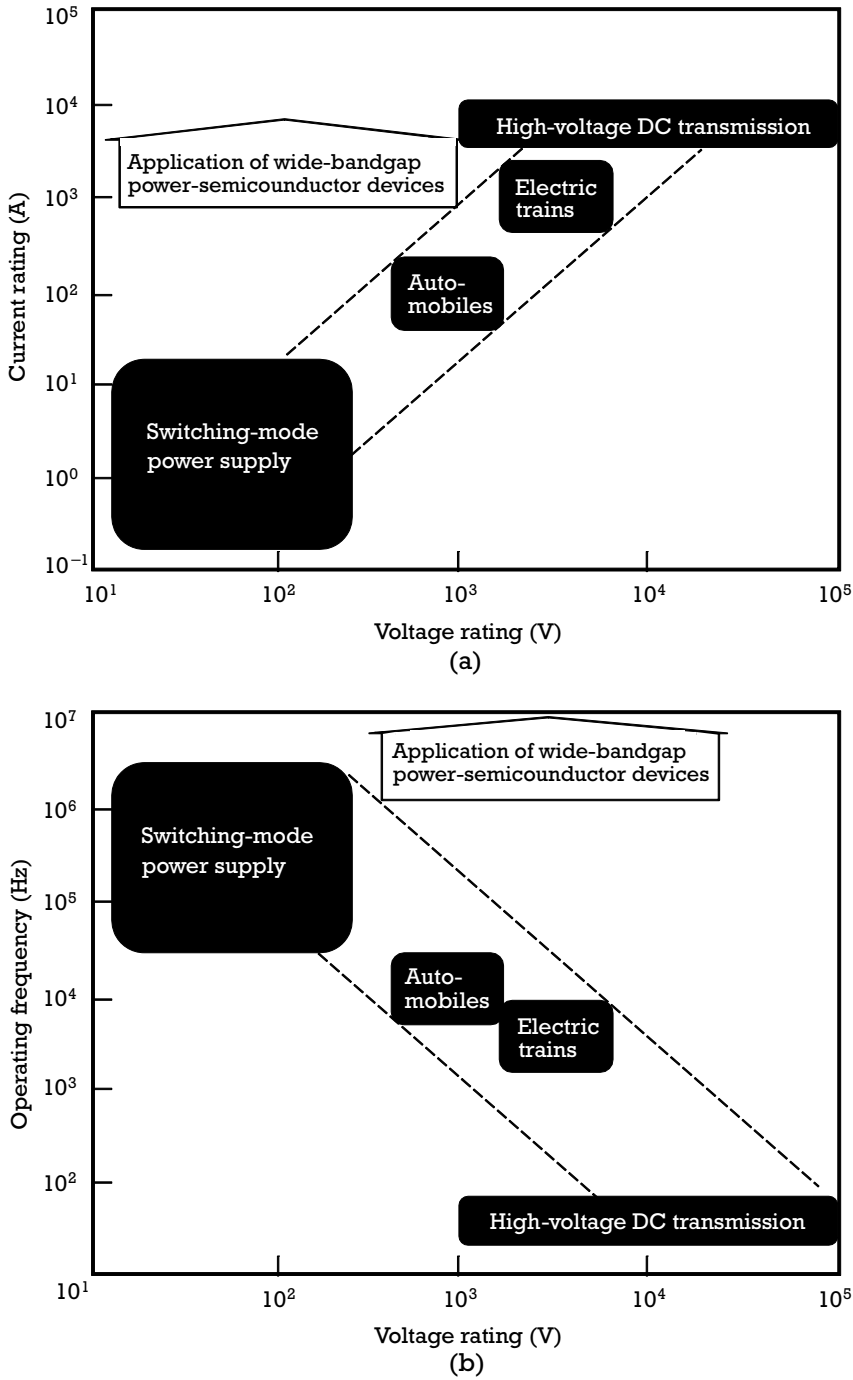

Figure 1.2 Applications of power-semiconductor devices from the viewpoints of (a) current rating and (b) operating frequency.

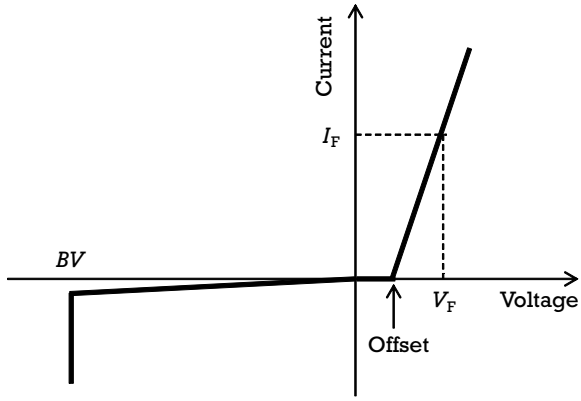

Figure 1.3 Schematic illustration of current/voltage characteristics of power-semiconductor diodes (I_F: forward current; V_F: forward-voltage drop; BV: breakdown voltage).

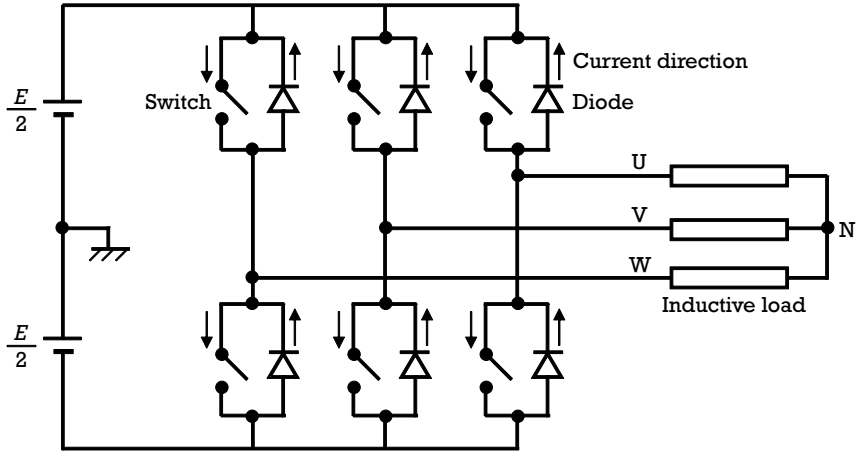

Figure 1.4 Circuit configuring a three-phase voltage-source inverter.

1.3 Vertical versus Lateral Unipolar Power Devices

In a semiconductor, current is carried by two types of carriers, namely, negatively charged electrons and positively charged holes. Power-semiconductor devices can thus be classified as unipolar and bipolar devices. In the case of unipolar devices, current is carried via electrons or holes; in bipolar devices, on the other hand, current is carried by both electrons and holes. As classified in Figure 1.6, lateral unipolar power-switching devices and lateral unipolar power diodes with structures comprising GaN layers on Si substrates, GaN layers on SiC substrates, GaN layers on sapphire substrates,

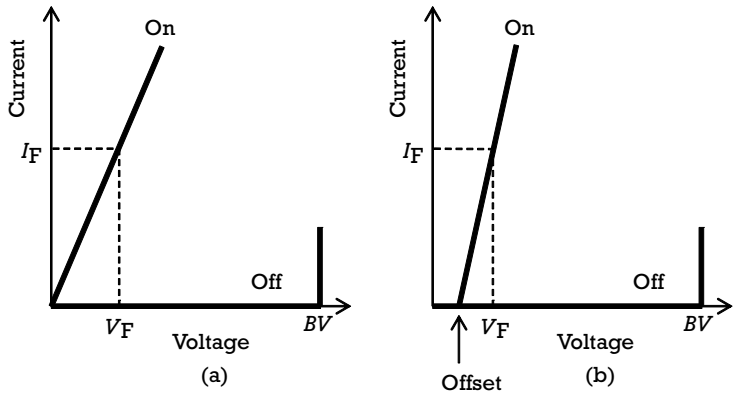

Figure 1.5 Schematic illustration of (a) zero-offset-voltage and (b) offset-voltage characteristics of power-semiconductor switching devices (I_F: forward current; V_F: forward-voltage drop; BV: breakdown voltage).

	Lateral power-switching device	Lateral power diode
Unipolar device	• GaN on Si substrate • GaN on SiC substrate • GaN on GaN substrate • GaN on sapphire substrate • SiC on SiC substrate	
Bipolar device	*Not widely used*	*Not widely used*

Figure 1.6 Classification of lateral power-switching devices and diodes as unipolar and bipolar devices.

GaN layers on GaN substrates, or SiC layers on SiC substrates have been reported; however, lateral bipolar power-switching devices and lateral bipolar power diodes have not been widely used. Therefore, this section compares vertical and lateral devices with respect to unipolar power-switching devices and unipolar power diodes.

1.3.1 Vertical versus Lateral Unipolar Power-Switching Devices

Figure 1.7 shows lateral and vertical unipolar power-switching devices with an area A of 1 cm^2. Unipolar power-switching devices show zero-offset-voltage characteristics, shown in Figure 1.5(a), where specific on-resistance $R_{on}A$ is defined as $V_F A/I_F$. Lateral unipolar power-switching devices gain an advantage over vertical ones in that $R_{on}A$ does not include specific substrate resistance $R_{sub}A$ (Figure 1.7[a]).

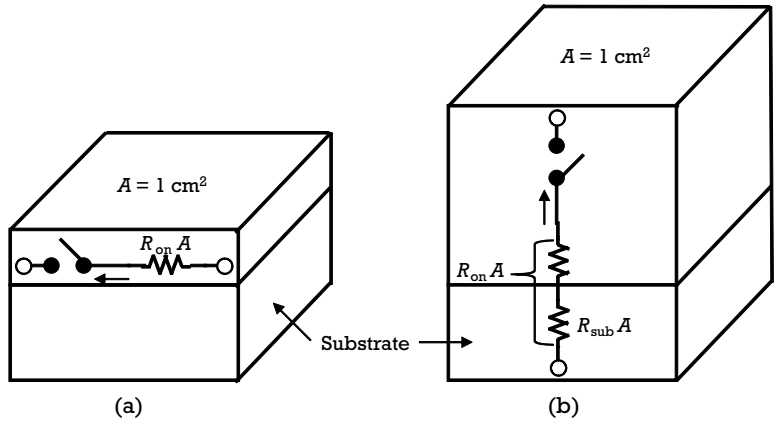

Figure 1.7 Schematic illustration of (a) lateral and (b) vertical unipolar power-switching devices with an area A of 1 cm^2, where $R_{on}A$ and $R_{sub}A$, respectively, denote specific on-resistance and specific substrate resistance.

1.3.1.1 Vertical versus Lateral GaN Unipolar Power-Switching Devices

In Figure 1.8, $R_{on}A$ of lateral GaN unipolar power-switching devices that have been manufactured [2] is plotted as a function of voltage rating. $R_{sub}A$ values of GaN and SiC substrates, which are also shown in Figure 1.8, are calculated as follows. The resistivity and thickness of GaN substrates are, respectively, reported to be 0.018 Ω cm and 600 μm [6], while those of SiC substrates are, respectively, reported to be 0.015–0.02 Ω cm and 350–500 μm [7]. $R_{sub}A$ values of GaN and SiC substrates are thus calculated, respectively,

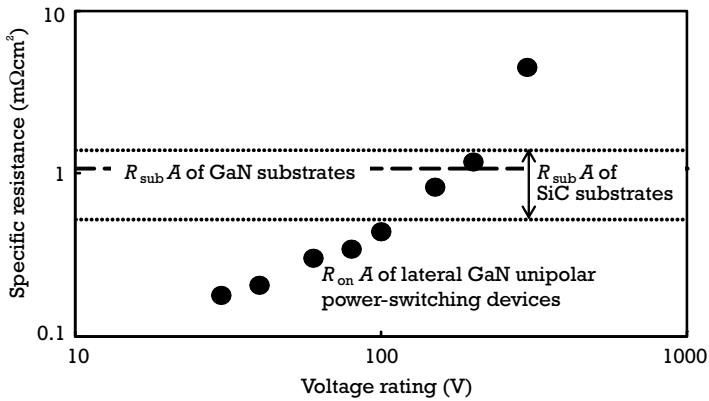

Figure 1.8 Voltage-rating dependence of reported room-temperature-specific on-resistance ($R_{on}A$) of lateral GaN unipolar power-switching devices [2], together with specific substrate resistance ($R_{sub}A$) of GaN (dashed line) and SiC substrates (dotted lines) [6, 7].

to be 1.1 (dashed line in Figure 1.8) and 0.53–1.4 mΩcm^2 (dotted lines in Figure 1.8). Moreover, $R_{on}A$ of lateral GaN unipolar power-switching devices increases with increasing voltage rating but does not exceed $R_{sub}A$ of GaN and SiC substrates as long as the voltage rating is less than 200V. Furthermore, as stated in Section 1.1, the previously fabricated lateral GaN unipolar switching-devices are formed on Si substrates [2], which are much cheaper and larger than GaN substrates. That means that lateral GaN unipolar power-switching devices are suitable for low-cost and low-voltage applications such as the switching-mode power supply shown in Figure 1.2.

With respect to a voltage rating exceeding about 400V, the maximum chip current of lateral GaN-on-Si-substrate unipolar power-switching devices is 70A (A = 0.29 cm^2) [8] (Figure 1.9). Because no larger currents have been reported since 2009, this value seems to be a practical limit. Uniform operation of lateral GaN unipolar power-switching devices on a larger GaN-

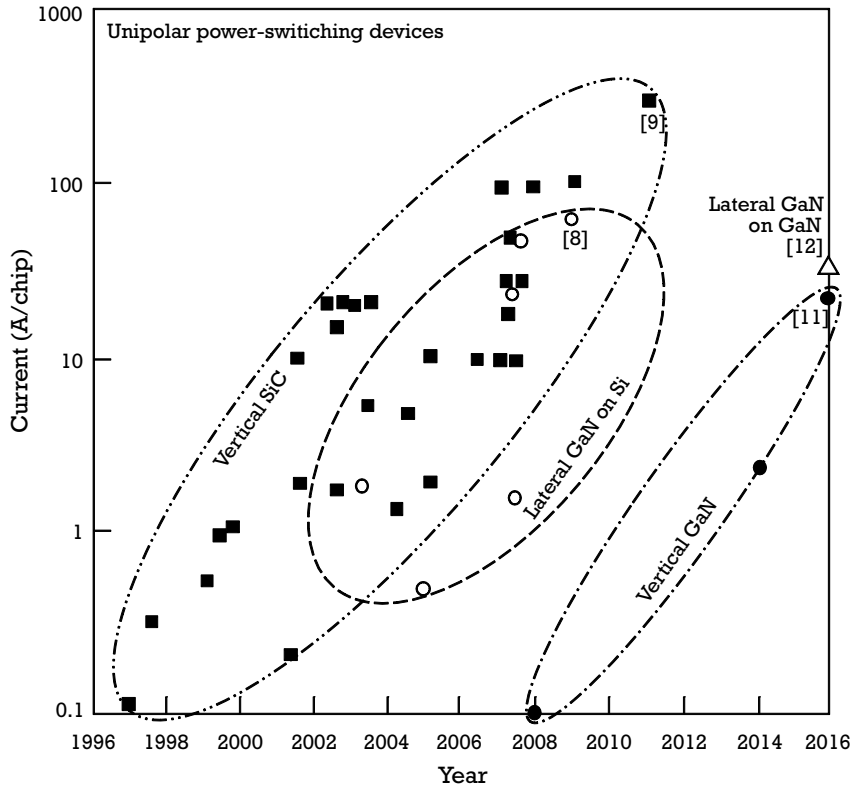

Figure 1.9 Reported current per chip of lateral GaN-on-Si substrate (open circles), lateral GaN-on-GaN substrate (open triangle), vertical GaN (solid circles), and vertical SiC (solid squares) unipolar power-switching devices as a function of the year of publication.

on-Si chip is probably prevented by the high density of crystalline defects (see Section 2.2.3) and residual stress in GaN layers on nonnative substrates.

On the other hand, vertical GaN unipolar power-switching devices are following the same trend as vertical SiC unipolar power-switching devices (up to 350A with A of 1.0 cm^2 [9]) but with a 10-year delay. In general, vertical power-switching devices have the advantage of having higher voltage at their bottom so that crossover metallization used in lateral power-switching devices can be eliminated [10]. A chip current of 23A (A = 0.023 cm^2) demonstrated in a vertical GaN unipolar power-switching device [11] is thus considered to increase up to about 350A. It is therefore clear that vertical GaN unipolar power-switching devices are desirable for large-current and high-voltage operation. Note here that the maximum chip current of lateral unipolar power-switching devices may become larger in the future since a newly developed lateral GaN unipolar power-switching device formed on a GaN substrate demonstrated 32A per chip with A of 0.040 cm^2 [12]. Note also, however, that the use of GaN substrates for lateral devices sacrifices the low cost expected in the case of lateral devices formed on Si substrates.

1.3.1.2 Vertical versus Lateral SiC Unipolar Power-Switching Devices

Figure 1.10 plots reported $R_{on}A$ values of lateral [13–19] and vertical [20–22] SiC unipolar power-switching devices as a function of breakdown voltage. The reported $R_{on}A$ of lateral SiC unipolar power-switching devices is more than 10 times higher than the reported $R_{on}A$ of vertical SiC unipolar power-switching devices. Although an approach to improving the poorer $R_{on}A/BV$ relation was proposed in 2005 [23], its effect has yet to be demonstrated. Therefore, vertical SiC unipolar power-switching devices are considered to be desirable for large-current and high-voltage operation, which is similar to the case of GaN unipolar power-switching devices (described in Section1.3.1.1).

1.3.2 Vertical versus Lateral Unipolar Power Diodes

Since few papers have been published on lateral unipolar SiC power diodes, only unipolar GaN power diodes are considered. Unlike power-switching devices, power diodes do not have control terminals. Therefore, in the case of lateral unipolar power diodes, multiple diodes can be connected in parallel (Figure 1.11); for example, up to eight parallel diodes (consisting of aluminum-gallium-nitride [AlGaN]/GaN heterojunction [24]) have been reported [25]. (Note that AlGaN is an alloy of aluminum nitride [AlN] and GaN.) Among those lateral unipolar power diodes, three parallel AlGaN/GaN diodes on Si

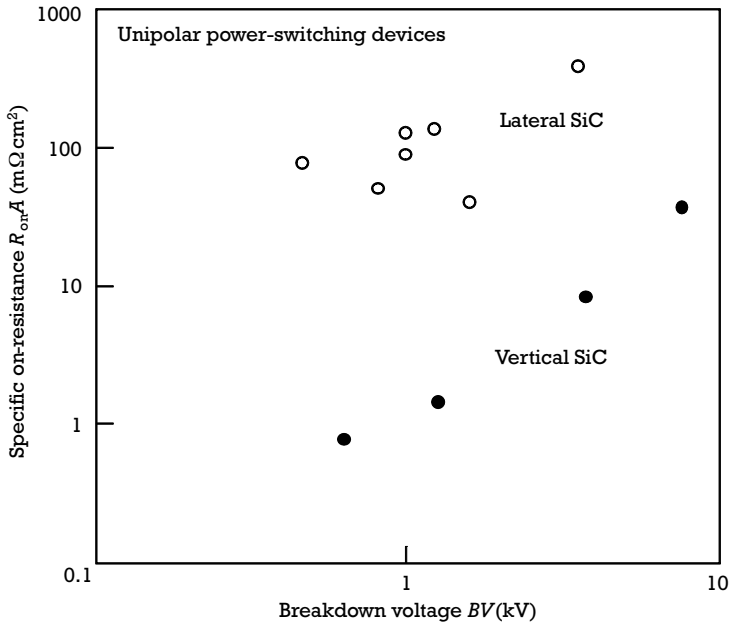

Figure 1.10 Reported room-temperature-specific on-resistance of lateral (open circles) [13–19] and vertical (solid circles) [20–22] SiC unipolar power-switching devices as a function of breakdown voltage.

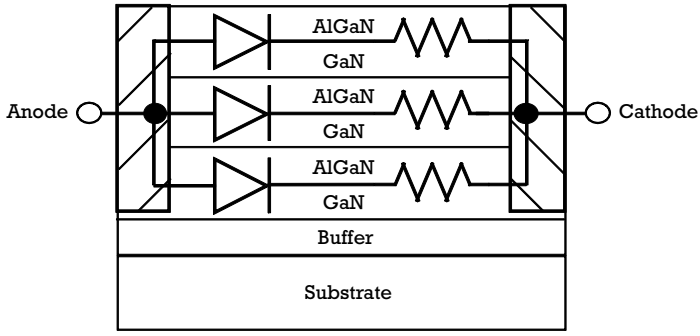

Figure 1.11 Schematic illustration of lateral unipolar power diodes comprising three parallel AlGaN/GaN heterojunction diodes.

substrates with breakdown voltages and chip sizes of, respectively, 600V and 3.4×4 mm, and a maximum chip current of 20A were reported [26].

Lateral and vertical unipolar power diodes with A of 1 cm^2 are schematically illustrated in Figure 1.12. Unipolar power diodes have offset-voltage characteristics as shown in Figure 1.3, where differential specific on-resistance $R_{on}A^{diff}$ is defined as $dV_F A/dI_F$. Lateral unipolar power diodes should

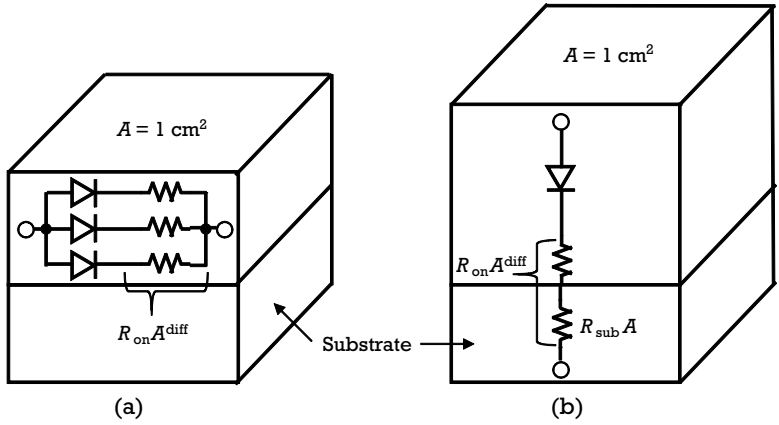

Figure 1.12 Schematic illustration of (a) lateral and (b) vertical unipolar power diodes with an area A of 1 cm^2, where $R_{on}A^{diff}$ and $R_{sub}A$, respectively, denote differential specific on-resistance and specific substrate resistance.

gain an advantage over vertical ones in that $R_{on}A^{diff}$ does not include $R_{sub}A$. Unlike lateral unipolar power-switching devices, however, lateral unipolar power diodes with a voltage rating of less than 200V have not been reported.

In the case of a voltage rating of about 600V, current-density/voltage characteristics of the above-described three parallel AlGaN/GaN diodes on Si substrates [26] are compared to those of the reported 790-V 50-A vertical GaN unipolar power diodes (with anode area of 3×3 mm) [27] (Figure 1.13). Since the chip size of the vertical GaN unipolar power diode is not described in [27], two probable sizes (minimum: 3.4×3.4 mm; maximum: 4×4 mm) are assumed in the calculation of its current density. Even in the case of assuming the larger chip size, the current density of the vertical GaN unipolar power diode is larger than that of the three parallel AlGaN/GaN diodes (Figure 1.13).

While the maximum chip current of lateral GaN unipolar power diodes [26] has not increased since 2011, the maximum chip current of vertical GaN unipolar power diodes is still increasing [27] and following the trend of vertical SiC unipolar power diodes [28], but with a delay of about 10 years (Figure 1.14).

1.4 Summary

This chapter briefly explains the functions of power-semiconductor switching devices and diodes through an example case of a three-phase voltage-source inverter. As materials for next-generation power-switching devices,

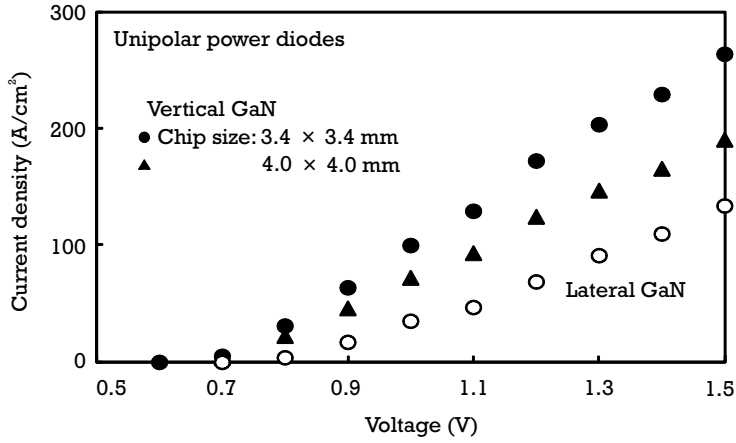

Figure 1.13 Current-density/voltage characteristics of large-current (> 20A) lateral GaN (open circles: chip size of 3.4 × 4 mm) [26] and vertical GaN (solid circles: probable minimum chip size of 3.4 × 3.4 mm; solid triangles: probable maximum chip size of 4 × 4 mm) [27] unipolar power diodes.

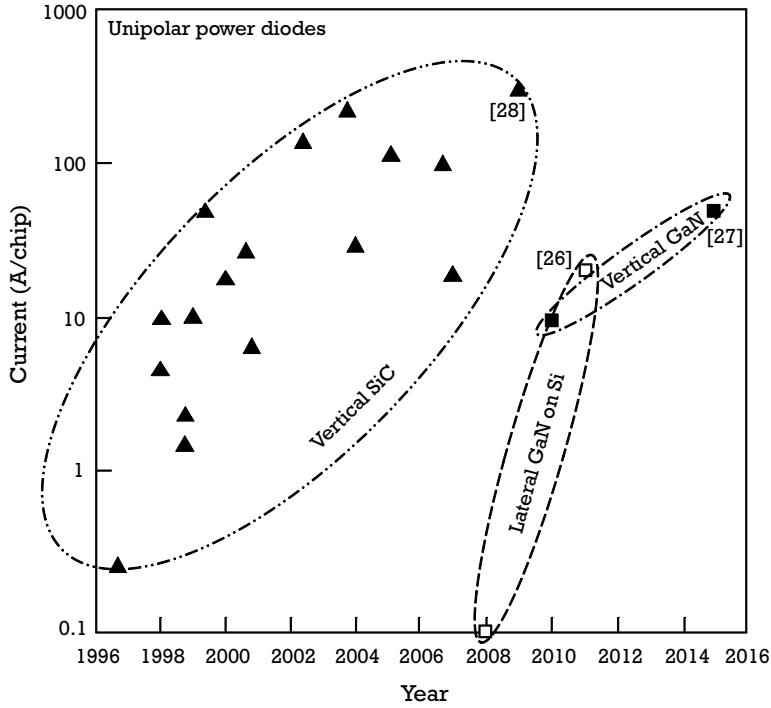

Figure 1.14 Reported current per chip of lateral GaN-on-Si substrate (open squares), vertical GaN (solid squares), and vertical SiC (solid triangles) unipolar power diodes as a function of the year of publication.

SiC and GaN are introduced as the most promising wide-bandgap semiconductors. With respect to vertical versus lateral device configuration, these materials are compared in the cases of unipolar power-switching devices and diodes. When the voltage rating is less than 200V, lateral unipolar GaN power-switching devices demonstrate their advantage in terms of lower $R_{on}A$; on the other hand, when the voltage rating exceeds 400V, vertical GaN and SiC power-switching devices and power diodes achieve larger maximum chip current and higher current density compared to lateral GaN ones. In accordance with these findings, the following chapters discuss only vertical power devices.

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CHAPTER

2

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2.3 Energy Bands

2.4 Impurity Doping

2.5 Carrier Mobility

2.6 Impact Ionization

2.7 Figure of Merit

2.8 Summary

Physical Properties of GaN and SiC

2.1 Introduction

As stated in Section 1.1, wide-bandgap semiconductors, such as GaN and SiC, have attracted great attention due to their superior material properties compared to silicon; however, neither GaN nor SiC exist in significant quantities in nature. While GaN was first synthesized in powder form by Maruska and Tietjen in 1969 [1], the first synthesis of SiC (in 1824) was reportedly accidental: the result of attempts by Berzelius to make diamond [2].

In fabrication of power devices based on GaN or SiC, a GaN or SiC layer is grown on a substrate (described in Section 1.3). The unavailability of GaN substrates forced early researchers to use sapphire substrates because the thermal-expansion coefficient of sapphire is relatively close to that of GaN. Since 1986, Akasaki, Amano, and their coworkers have improved the quality of GaN layers by inserting an AlN nucleation layer between the GaN layer and the sapphire substrate [3, 4]. In 1988, they achieved p-type doping, which introduces

holes (i.e., positively charged carriers [see Section 1.3]), in GaN [5]. The first development of practical GaN optical devices (namely, p-n junction blue-light-emitting diodes fabricated by Nakamura et al. in 1991 [6]) was followed by the first demonstration of a GaN electron device on a sapphire substrate in 1993 [7]. A large lattice misfit of about 13% at growth temperature [8], however, generated a high density of crystalline defects (namely, dislocations, as described in Section 2.2.3) in GaN layers grown on sapphire substrates. In 1999, two-inch freestanding GaN substrates were produced from 250–300-μm thick GaN films grown on sapphire [9]. Since then, vertical GaN power devices have been fabricated [10], and electrical characterization of GaN layers with a low density of defects have been investigated [11].

In contrast to GaN, SiC has been mainly used as a substrate for growing a SiC layer, since a technique for seeded sublimation called the modified Lely method was developed by Tairov and Tsvetkov in 1978 [12]. Sublimation was needed because the solubility of carbon in silicon solution is low (e.g., only 0.1% carbon can be dissolved in silicon at 2,073– 2,273K [13]). In contrast to p-type doping in GaN, p-type doping in SiC has not been difficult. However, growing a SiC layer had been difficult because of the tendency of SiC to crystallize into over 250 modifications (so-called polytypes) [14]. In 1987, Kuroda et al. proposed a technique called step-controlled epitaxy [15] to reproduce the same polytype in a SiC layer as that in the substrate it is grown on. Note that the term epitaxy, which means a crystalline overlayer having well-defined orientation with respect to the substrate crystal structure (see Chapter 6), comes from two Greek words: epi meaning upon and taxis meaning arrangement. Owing to the above two techniques, the opportunity to fabricate and apply SiC power devices grew ripe in the early 1990s [16].

In view of the above-described history concerning GaN and SiC, the remainder of this chapter compares crystal structures, including crystal defects, of GaN and SiC and then describes their energy bands, impurity doping, carrier mobility, and impact ionization. Since some vertical GaN power-switching devices utilize AlGaN/GaN heterostructures [17–19], crystal structures and energy bands of AlN are also described. Finally, Section 2.7 introduces a commonly used figure of merit for power devices.

2.2 Crystal Structures

AlN, GaN, and SiC are compound semiconductors that allow a stoichiometry of 50% aluminum, gallium, or silicon and 50% nitrogen or carbon. Note that silicon germanium ($Si_{1-x}Ge_x$) is not a compound semiconductor but an alloy semiconductor because x can take any value from 0 to 1. The

electronic structures of aluminum, gallium, nitrogen, silicon, and carbon atoms in their ground states are as follows:

$$_{13}\text{Al: } 1s^2\ 2s^2\ 2p^6\ 3s^2\ 3p^1 \tag{2.1a}$$

$$_{31}\text{Ga: } 1s^2\ 2s^2\ 2p^6\ 3s^2\ 3p^6\ 3d^{10}\ 4s^2\ 4p^1 \tag{2.1b}$$

$$_{7}\text{N: } 1s^2\ 2s^2\ 2p^3 \tag{2.1c}$$

$$_{14}\text{Si: } 1s^2\ 2s^2\ 2p^6\ 3s^2\ 3p^2 \tag{2.1d}$$

$$_{6}\text{C: } 1s^2\ 2s^2\ 2p^2 \tag{2.1e}$$

where the subscripts and the superscripts, respectively, show atomic number and number of orbital electrons. Both aluminum and gallium have three valence electrons in their outermost shells, while nitrogen has five valence electrons in its outermost shells. AlN and GaN are thus known as III-V compound semiconductors. On the other hand, SiC is called a IV-IV compound semiconductor because both silicon and carbon have four valence electrons in their outermost shells.

2.2.1 Crystal Structures of AlN and GaN

AlN and GaN can take any of the following crystalline structures: rock salt (Figure 2.1), zincblende (Figure 2.2[a]), or wurtzite (Figure 2.2[b]). Rock-salt structures are observed under very high pressures only: 23 GPa for AlN [20] and 52 GPa for GaN [21]. Under ambient conditions, the thermodynamically stable structure for both AlN and GaN is wurtzite. The energy differences for various compound semiconductors (calculated using wave-function and classical-orbital radii [22]) are plotted in Figure 2.3. In

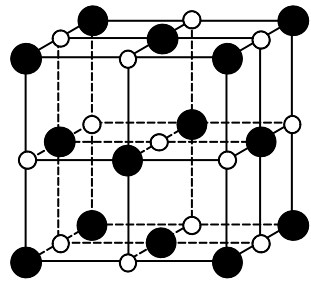

Figure 2.1 Rock-salt crystal structure (solid circles: aluminum and/or gallium atoms; open circles: nitrogen atoms).

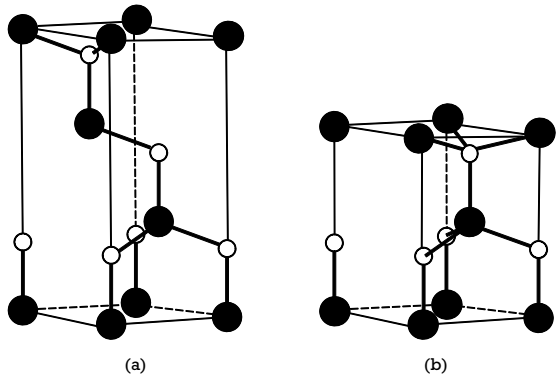

Figure 2.2 (a) Zincblende and (b) wurtzite crystal structures (solid circles: aluminum and/or gallium atoms; open circles: nitrogen atoms).

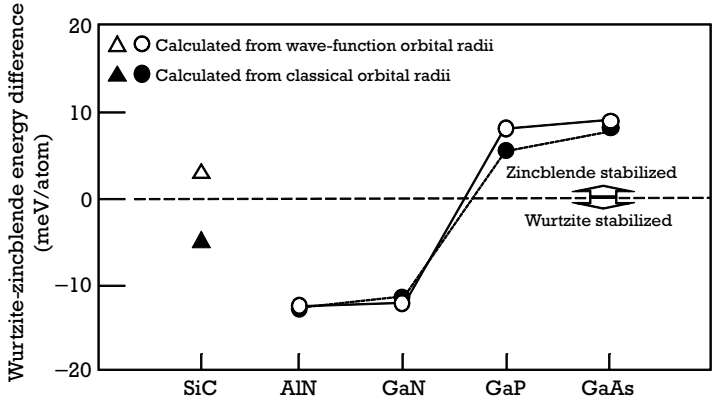

Figure 2.3 Calculated energy differences for wurtzite-zincblende structures [22].

contrast to zincblende-stabilized III-V compound semiconductors, such as gallium phosphide (GaP) and gallium arsenide (GaAs), both AlN and GaN are wurtzite-stabilized III-V compound semiconductors. Note that it is not clear from Figure 2.3 whether SiC is a zincblende-stabilized or wurtzite-stabilized IV-IV compound semiconductor; experimentally, however, as described in Section 2.2.2, zincblende SiC often appears at relatively low temperature

Plan and perspective views of the wurtzite structure [Figure 2.2(b)] are shown in Figure 2.4. In such hexagonal-prism crystals, crystal planes can be expressed with Miller-Bravais indices (*hkil*) [23] such that the relation

$$h + k + i = 0 \tag{2.2}$$

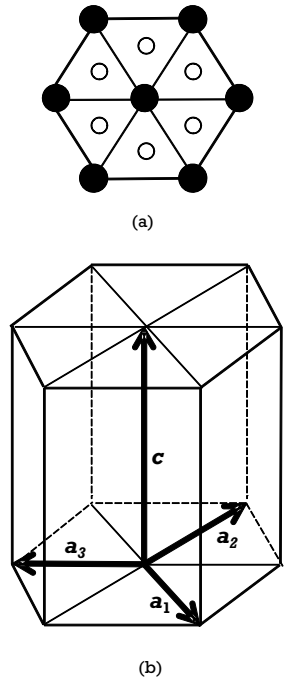

Figure 2.4 (a) Plan and (b) perspective views of the wurtzite structure shown in Figure 2.2(b) (solid circles: aluminum and/or gallium atoms; open circles: nitrogen atoms).

is always satisfied. The indices are determined by performing the following steps:

- Determining the intercepts of the plane with the a_1, a_2, a_3, and c axes;
- Forming the reciprocals of the intercepts;
- Finding the smallest set of integers that are in the same ratio as the intercepts;
- Writing the indices with a bar if they are negative.

Typical crystal planes in the wurtzite structure are shown in Figure 2.5. The (0001) plane (which features aluminum and/or gallium polarity (Figure 2.6[a]) shown in Figure 2.5(a) is the most common substrate-surface for GaN power devices [9]. The following substrates have also been fabricated: $(000\bar{1})$ which features nitrogen polarity (Figure 2.6[b]) GaN [24], $(10\bar{1}0)$ so-called *m*-plane GaN [25], $(11\bar{2}0)$ so-called *a*-plane GaN [26], (0001) AlN [27], $(10\bar{1}0)$ AlN [28], and (0001) AlGaN [29].

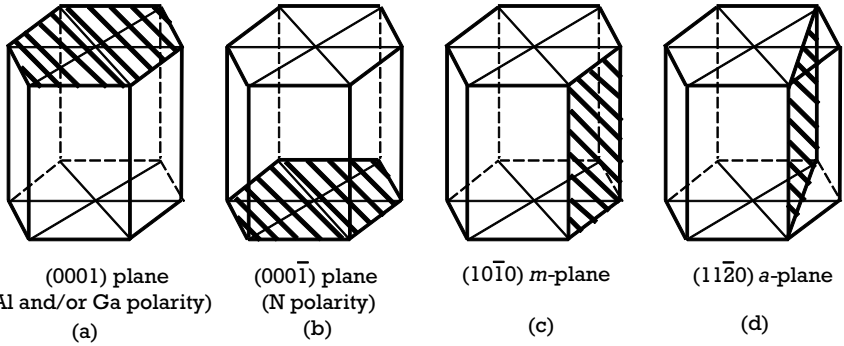

Figure 2.5 Typical crystal planes in the wurtzite structure shown in Figures 2.2(b) and 2.4.

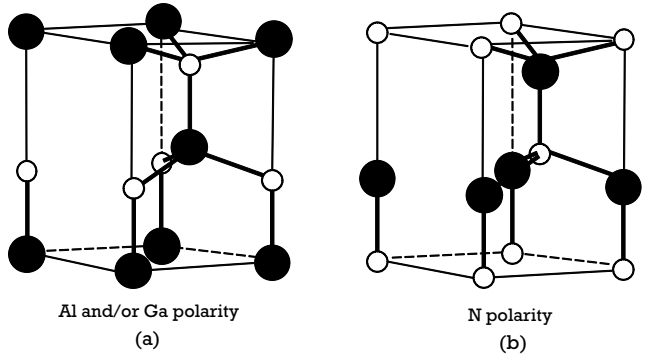

Figure 2.6 Atomic arrangement of (a) (0001) and (b) (000 $\bar{1}$) planes in the wurtzite structure shown in Figure 2.5(a, b) (solid circles: aluminum and/or gallium atoms; open circles: nitrogen atoms).

2.2.2 Crystal Structures of SiC

Polytypes are expressed with the number of Si-C stacking layers in a unit cell and the crystal system (e.g., C for cubic and H for hexagonal). The atomic arrangements of common polytypes (i.e., 3C-, 4H-, and 6H-SiC), together with those of 2H-SiC, are shown in Figure 2.7, where A, B, and C are the occupation sites in a hexagonal close-packed structure (Figure 2.8). 3C-SiC (i.e., zincblende SiC) is a low-temperature stable polytype that is transformed into hexagonal polytypes above 2,300K [30]. 2H-SiC (i.e., wurtzite SiC) is also unstable at high temperatures. As a power semiconductor, 4H-SiC is superior to 6H-SiC because electron transport in 6H-SiC strongly depends on crystallographic orientations (see Section 2.5).

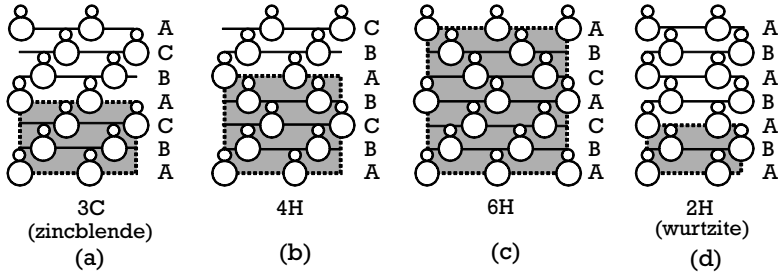

Figure 2.7 Schematic cross-sections of common polytypes of (a) 3C-SiC, (b) 4H-SiC, (c) 6H-SiC, and (d) 2H-SiC. Large and small circles denote silicon and carbon atoms, respectively.

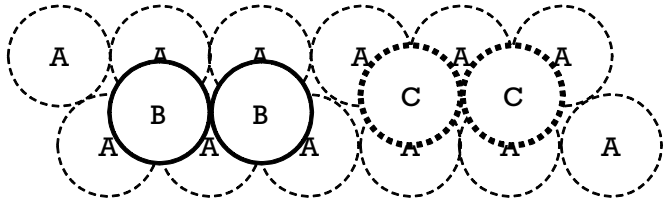

Figure 2.8 Schematic plan view of occupation sites (A, B, and C) in the hexagonal close-packed structure.

Note that in accordance with the above definition, zincblende and wurtzite GaN (or AlN) can be expressed as 3C- and 2H-GaN (or AlN). For simplicity, however, GaN (or AlN) hereinafter means the most stable wurtzite GaN (or AlN).

2.2.3 Crystal Defects

Some crystal defects are electrically active and are thus of major concern for power devices. In general, they can be categorized as four types: zero-dimensional (i.e., point), one-dimensional (i.e., line), two-dimensional (i.e., areal), and three-dimensional (bulk) defects.

Point defects influence carrier lifetime (see Chapter 3) and, consequently, conductivity modulation in bipolar devices (see Section 3.7). Two basic types of native point defects are well-known: vacancies (also known as Schottky defects) (i.e., atoms missing from lattice sites) and interstitials (also known as Frenkel defects) (i.e., additional atoms in between lattice sites) [31]. In thermal equilibrium, the concentrations of vacancies (C_V) and interstitials (C_I) take equilibrium values (C_V^* and C_I^*, respectively) that are determined from the respective free energies of formation, F_V and F_I, as follows [32, 33]:

$$C_V^* = C_{sV} \exp(-F_V/kT) \tag{2.3a}$$

$$C_I^* = C_{sI} \exp(-F_I/kT) \tag{2.3b}$$

where C_{sV} and C_{sI} are, respectively, the concentrations of the sites that are open to vacancies and interstitials, k is Boltzmann's constant, and T is absolute temperature. In the case of silicon, $C_{sV} = 2.0 \times 10^{23}$ cm^{-3}, $F_V = 2.0$ eV, $C_{sI} = 5.0 \times 10^{22}$ cm^{-3}, and $F_I = 2.36$ eV have been conventionally used in a commercial process simulator [34]. These values were successfully applied for boron diffusion in 4H-SiC (see Section 7.4), even though the exact values for GaN and 4H-SiC are unknown. Other than general vacancies and interstitials, carrier traps in GaN have been investigated [35] and the reported results on two major point defects (i.e., $Z_{1/2}$ [36] and $EH_{6/7}$ [37]) in 4H-SiC have been summarized [38].

Line defects are called dislocations. Edge (Figure 2.9[a]) and screw dislocations (Figure 2.9[b]) are the two primary types of dislocations, while mixed dislocations are intermediate between these dislocations. An edge dislocation is formed when an extra (or missing) half-plane of atoms is introduced. In Figure 2.9(a), the dislocation lying in the basal plane (i.e., [0001]) is called a basal-plane dislocation (BPD); the dislocation lying perpendicular to (0001) is called a threading edge dislocation (TED). The difference between a BPD and a TED is only the direction of the dislocation; thus, a BPD often converts to a TED and vice versa. With respect to screw dislocations, a threading dislocation (solid line in Figure 2.9[b]) becomes an origin of spiral growth (see Sections 6.2, 6.4, and 6.5). Note, however, that in the case of GaN and 4H-SiC, the height of the spiral step differs: one Ga-N bilayer in the case of GaN and four Si-C bilayers in the case of 4H-SiC. Since threading dislocations act as nonradiative recombination centers (see Section 3.4.2) in GaN [39], they directly affect performance of GaN-based light emitters, especially laser diodes (LDs). The use of GaN substrates, instead of sapphire substrates, reduced the density of threading dislocations to the order of 10^6 cm^{-2}, thereby improving the reliability of GaN LDs. Threading dislocations similarly influence carrier lifetime in GaN and 4H-SiC bipolar power devices locally, but they do not influence carrier lifetime in unipolar power devices [38].

Areal defects that alter the periodic sequence of layers are called stacking faults (Figure 2.10). In GaN, stacking faults are rarely observed because stacking-fault energy is high (1.2 J/m^2) [40]. Furthermore, theory suggests that stacking faults in GaN are not electrically active [41]. In 4H-SiC, on the other hand, stacking faults are common defects because stacking-fault energy is low (0.014 J/m^2) [42].

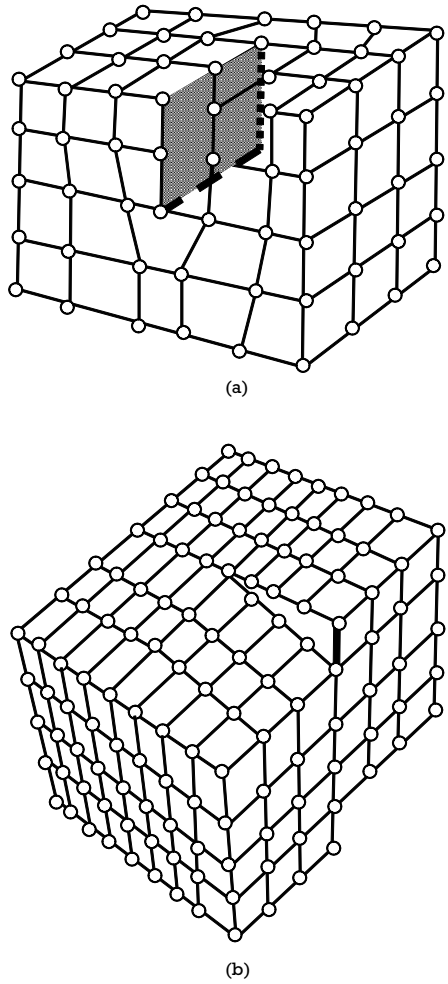

Figure 2.9 Schematic illustration of (a) edge and (b) screw dislocations. In (a), an extra half-plane is inserted. When the surface in (a) is (0001), the dashed line is a basal plane dislocation and the dotted line is a threading-edge dislocation.

So-called inversion domains are also known as areal defects in GaN. Inversion domains have opposite growth polarity to that of the matrix. In the case of a (0001) surface, V-shape pits are formed in inversion domains because GaN having nitrogen-polarity grows slower than GaN having gallium-polarity [43]. Inversion domains combined with strain change the piezoelectric field [44], and that change possibly affects the characteristics of vertical GaN power-switching devices with AlGaN/GaN heterostructures [17–19].

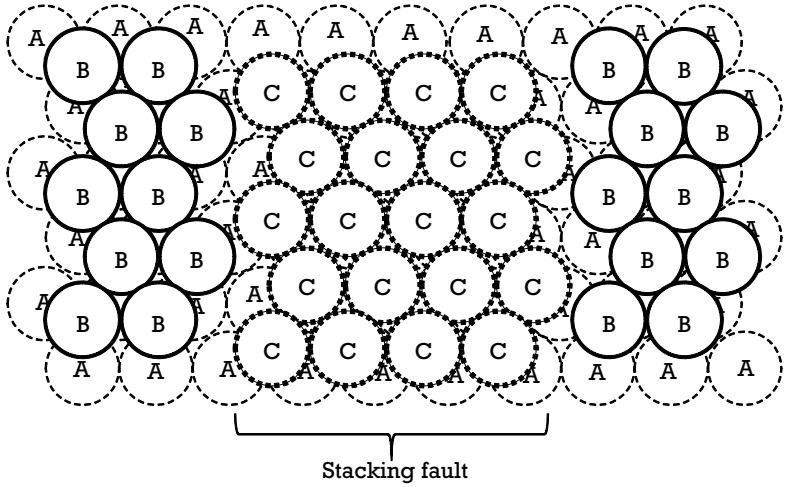

Figure 2.10 Schematic plan view of occupation sites (B) and stacking-fault sites (C) on occupation sites (A).

Bulk defects are associated with a volume including voids, cracks, and/or nano/micropipes. Nanopipes in GaN and micropipes in 4H-SiC are tunnel-like defects (i.e., open-core screw dislocations) aligned in the growth direction of the crystal, and they penetrate the film. In the case of epitaxial growth of 4H-SiC, micropipes were reported to be dissociated into multiple closed-core screw dislocations, leading to closure of micropipes [45, 46].

2.3 Energy Bands

An electron acted on by the coulombic potential of an atomic nucleus is allowed at certain energy levels only. As more atoms are added to form a crystal, the forces exerted on each electron are altered. Since the Pauli exclusion principle states that each allowed electron energy level has to be different, the original energy level splits into N different allowed levels when N atoms are added. Since the original energy level is in the order of a few electronvolts, and N is in the order of 10^{22}, the separation between the N different energy levels is in the order of 10^{-22} eV. This energy-level separation is so small (compared to thermal energy in the order of 10^{-2} eV) that electrons can easily move between the levels. The N different energy levels can therefore be regarded as a continuous band of allowed energies (i.e., an energy band).

In semiconductors, the valence electrons in the outermost shell completely fill an allowed energy band (i.e., the valence band), and an energy gap to the next-higher band exists (Figure 2.11). At temperatures above 0K,

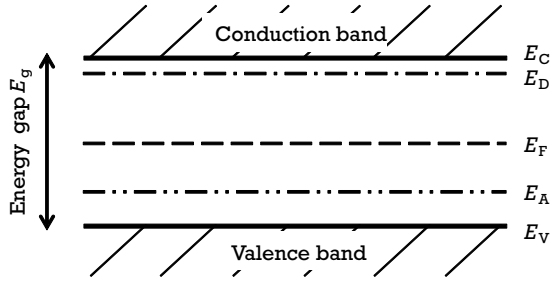

Figure 2.11 Energy bands for a semiconductor [bottom edge of the conduction band (E_C), donor level (E_D), Fermi level (E_F), acceptor level (E_A), and top edge of the valence band (E_V)].

the valence band is not entirely filled because a small number of electrons possess enough thermal energy to be excited across the energy gap into the next allowed band. Since the electrons in the upper band can respond to an applied electric field to produce current, the upper band is called the conduction band. The bottom edge of the conduction band and the top edge of the valence band are usually expressed as E_C and E_V, respectively.

When electrons are excited into the conduction band, empty states are left in the valence band. If an electric field is applied, nearby electrons can move into those empty states and produce current. The motion of charge in the valence band can thus be expressed in terms of the vacant states by treating the states as particles with positive charge. These particles are called holes (described in Section 1.3), whose concept can be understood through the analogy of bubbles in running water.

In semiconductors, E_C and E_V are functions of crystal momentum, and the energy gap E_g is defined as the difference between the minimum E_C and the maximum E_V (Figure 2.12). In the case of direct-bandgap semiconductors (e.g., AlN and GaN), the momentum at which E_C reaches a minimum and the momentum at which E_V reaches a maximum are the same (Figure 2.12[a]); however, in the case of indirect-bandgap semiconductors (e.g., silicon and SiC), they are different (Figure 2.12[b]).

In (a), an electron can shift from the highest-energy state in the valence band to the lowest-energy state in the conduction band without a change in crystal momentum. In (b), an electron cannot shift from the highest-energy state in the valence band to the lowest-energy state in the conduction band without a change in crystal momentum. Energies denoted by the solid vertical arrow come from photons (i.e., a quantum of electromagnetic radiation), while energy denoted by the dotted horizontal arrow comes from a phonon (i.e., an excited state in the quantum-mechanical quantization of the modes of vibrations).

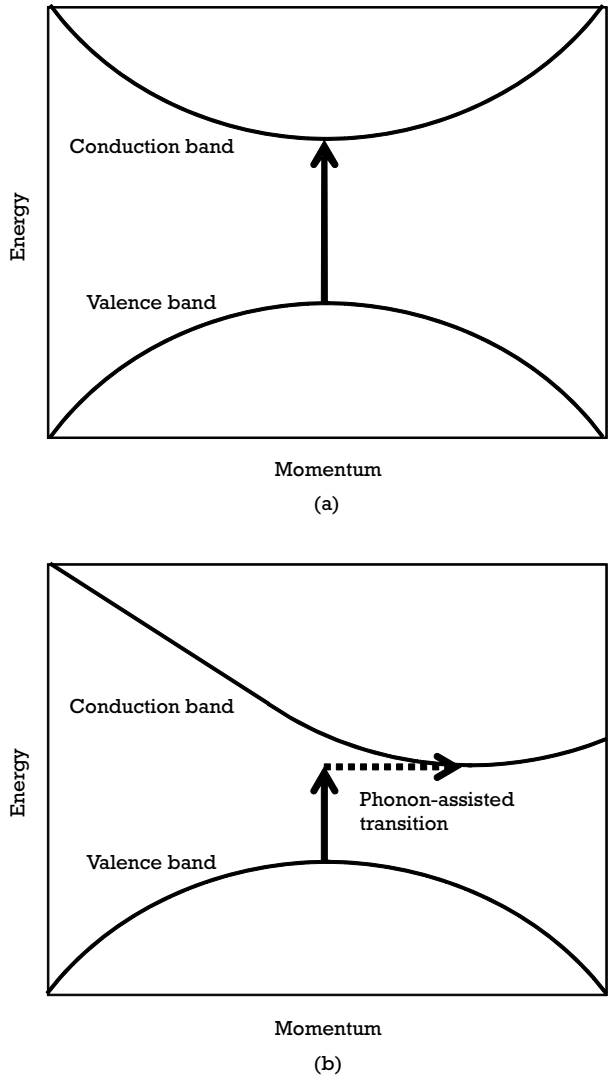

Figure 2.12 Energy versus crystal momentum for semiconductors with (a) direct bandgap and (b) indirect bandgap.

E_g can be obtained by optical absorption spectroscopy [31], in which optical-absorption coefficient α (cm^{-1}) is the most important parameter. The intensity of light, I_0, exponentially decreases to $I(x)$ at depth x from the surface as

$$I(x) = I_0 \exp(-\alpha x) \tag{2.4}$$

In direct-bandgap semiconductors, α is empirically known to be proportional to $(E_{photon}-E_g)^{0.5}$, where E_{photon} is the energy of a photon. The square root of the reported values of α [47–49] is thus plotted in Figure 2.13 as a function of E_{photon}. In the case of AlN and GaN, the onset of absorption is steep, and the threshold of absorption determines E_g. In the case of 4H-SiC, on the other hand, optical absorption slowly increases, even when E_{photon} exceeds E_g. Such different optical-absorption behaviors lead to photon recycling playing either a dominant or a negligible role (see Chapter 4).

2.4 Impurity Doping

The most useful means of controlling the number of carriers is incorporating substitutional impurities called dopants, namely, donors that donate electrons to conduction bands or acceptors that accept electrons from (and leave holes) in valence bands. If most of the dopants are donors, the semiconductor is called n-type; on the other hand, if most of the dopants are acceptors, the semiconductor is called p-type.

In intrinsic (i.e., nondoped) semiconductors, all carriers result from excitation across E_g. Consequently, electron concentration n and hole concentration p equal intrinsic carrier concentration n_i. The mass-action law, namely,

$$np = n_i^2 \tag{2.5}$$

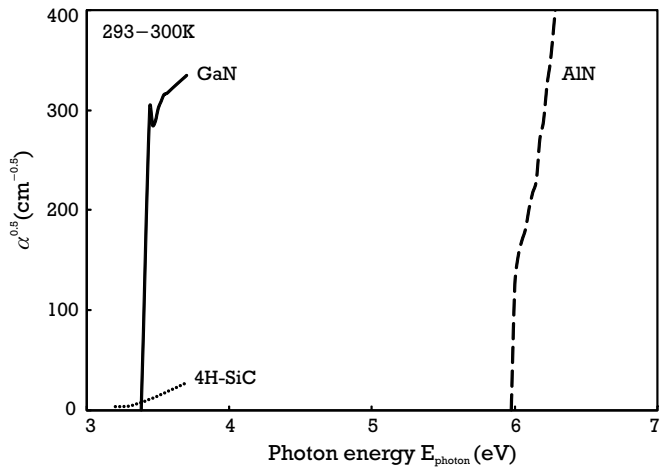

Figure 2.13 Square root of reported optical-absorption coefficients of AlN, GaN, and 4H-SiC as a function of photon energy [47–49].

gives n_i as

$$n_i = (N_C N_V)^{0.5} \exp(-E_g/2kT) \tag{2.6a}$$

$$N_C = 2\ (2\pi m_n kT/h^2)^{1.5} \tag{2.6b}$$

$$N_V = 2\ (2\pi m_p kT/h^2)^{1.5} \tag{2.6c}$$

where N_C and N_V are, respectively, effective density of states in conduction bands and valence bands; m_n and m_p denote, respectively, effective masses of electrons and holes; and h is Planck's constant. While N_C and N_V vary in proportion to $T^{1.5}$, n_i is much more temperature-dependent due to the exponential term in (2.6a). For GaN with E_g = 3.44 eV [50] and 4H-SiC with E_g = 3.23 eV [51], n_i doubles about every 3-K increase in temperature near room temperature. Dependences of n_i on T for GaN and 4H-SiC are expressed as [52, 53]:

$$\begin{aligned} n_i^{GaN} &= (4.3 \times 10^{14} \times T^{1.5} \times 8.9 \times 10^{15} \times T^{1.5})^{0.5} \\ &\quad \times \exp(-3.44 \times 1.6 \times 10^{-19}/2/1.38 \times 10^{-23}/T) \\ &= 2.0 \times 10^{15} T^{1.5} \exp(-2.0 \times 10^4/T)\ (\text{cm}^{-3}) \end{aligned} \tag{2.7a}$$

and

$$\begin{aligned} n_i^{4H\text{-}SiC} &= (3.25 \times 10^{15} \times T^{1.5} \times 4.8 \times 10^{15} \times T^{1.5})^{0.5} \\ &\quad \times \exp\ (-3.23 \times 1.6 \times 10^{-19}/2/1.38 \times 10^{-23}/T) \\ &= 3.9 \times 10^{15} T^{1.5} \exp(-1.9 \times 10^4/T)\ (\text{cm}^{-3}) \end{aligned} \tag{2.7b}$$

and they are shown in Figure 2.14 in comparison with the dependence of n_i on T for silicon. For example, at 150°C, n_i in Si reaches 10^{13} cm^{-3}, which is the practically minimum doping level. In GaN and 4H-SiC, on the other hand, n_i is far below that level even at 250°C. This lower n_i is the reason GaN and 4H-SiC power devices can operate at a much higher temperature.

2.4.1 n-Type Doping

As donors, silicon is used for GaN, while nitrogen or phosphorus is used for 4H-SiC. While a large amount of energy (exceeding E_g) is required to excite an electron from the valence band to the conduction band, only a small amount of energy is required to excite an electron from a donor to the conduction band. This requirement corresponds to a donor level E_D being located just below E_C (Figure 2.11). The reported minimum ionization

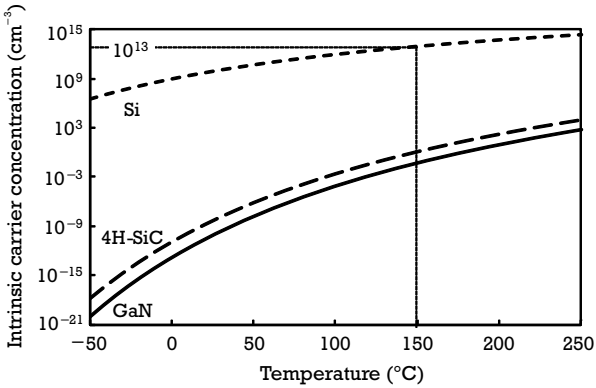

Figure 2.14 Temperature dependences of intrinsic carrier concentration in GaN, 4H-SiC, and silicon.

energy for donors (i.e., E_C–E_D) is 0.02 eV for silicon in GaN [51] and 0.059 eV for nitrogen in 4H-SiC [54].

At room temperature, these ionization energies are comparable to thermal energy (i.e., 0.026 eV), so all the donors (with concentration N_D) are considered to be ionized. The charge-neutrality condition in an n-type semiconductor is thus expressed as

$$N_D+p = n \tag{2.8}$$

Combining (2.5) with (2.8) leads to the following equation:

$$n^2+N_D n-n_i^2 = 0 \tag{2.9}$$

The positive solution of (2.9) under the condition $N_D >> n_i$ is

$$n = [-N_D+(N_D{}^2+4n_i^2)^{0.5}]/2 \approx N_D \tag{2.10}$$

2.4.2 p-Type Doping

As acceptors, magnesium is used for GaN, while aluminum or boron is used for 4H-SiC. Unlike E_D, acceptor level E_A is relatively far from E_V (Figure 2.11). Reported acceptor ionization energy (i.e., E_A–E_V) is about 0.2 eV for magnesium in GaN [55]; 0.2 eV for aluminum; and 0.3 eV for boron in 4H-SiC [56]. Since these values are much larger than thermal energy at the practically highest temperature (e.g., 0.045 eV at 250°C), not all acceptors are ionized. Concentration of ionized acceptors is given by [57]

$$N_A^- = N_A/\{1+4\ \exp[(E_A-E_F)/kT]\} \tag{2.11}$$

where N_A is acceptor concentration and E_F is the Fermi level (i.e., the energy level of an electron at thermodyanmic equilibrium with 50% probability of being occupied).

Since electron and hole concentrations are expressed as [57]

$$n = N_C\ \exp[-(E_C-E_F)/kT] \tag{2.12a}$$

and

$$p = N_V\ \exp[-(E_F-E_V)/kT] \tag{2.12b}$$

the charge-neutrality condition in a p-type semiconductor is expressed as

$$\begin{aligned} N_V\ \exp[-(E_F - E_V)/kT] &= N_A/\{1 + 4\ \exp[(E_A - E_F)/kT]\} \\ &\quad + N_C\ \exp[-(E_C - E_F)/kT] \\ &\approx N_A/\{1 + 4\ \exp[(E_A - E_F)/kT]\} \end{aligned} \tag{2.13}$$

From (2.13), E_F can be graphically determined, as shown in the examples for p-type GaN in Figure 2.15. Note that the acceptor ionization ratio r_A (i.e., N_A^-/N_A) depends not only on T but also on N_A (e.g., at $T = 150°C$, $r_A = 8.6\%$ when $N_A = 1\times10^{19}$ cm^{-3}, while $r_A = 58\%$ when $N_A = 1 \times 10^{17}$ cm^{-3}, as shown in Figure 2.15[b]).

2.5 Carrier Mobility

Drift velocity v_{drift} is defined as net carrier velocity in applied electric field E. Electrons are accelerated in the field direction during the time between their collisions with the crystal lattice. When colliding, electrons exchange energy with the lattice. As long as $|E|$ is small, however, the energy exchanged is small and the lattice is not heated appreciably. If the elementary charge (1.6×10^{-19} C) is denoted by q, the force on an electron is $-qE$ and the momentum gained is $m_n v_{drift}$, so the equation

$$-qE\tau = m_n v_{drift} \tag{2.14}$$

is satisfied for mean scattering time τ. Therefore, v_{drift} is given by

$$v_{drift} = -\mu_n E \tag{2.15a}$$

$$\mu_n = q\tau/m_n \tag{2.15b}$$

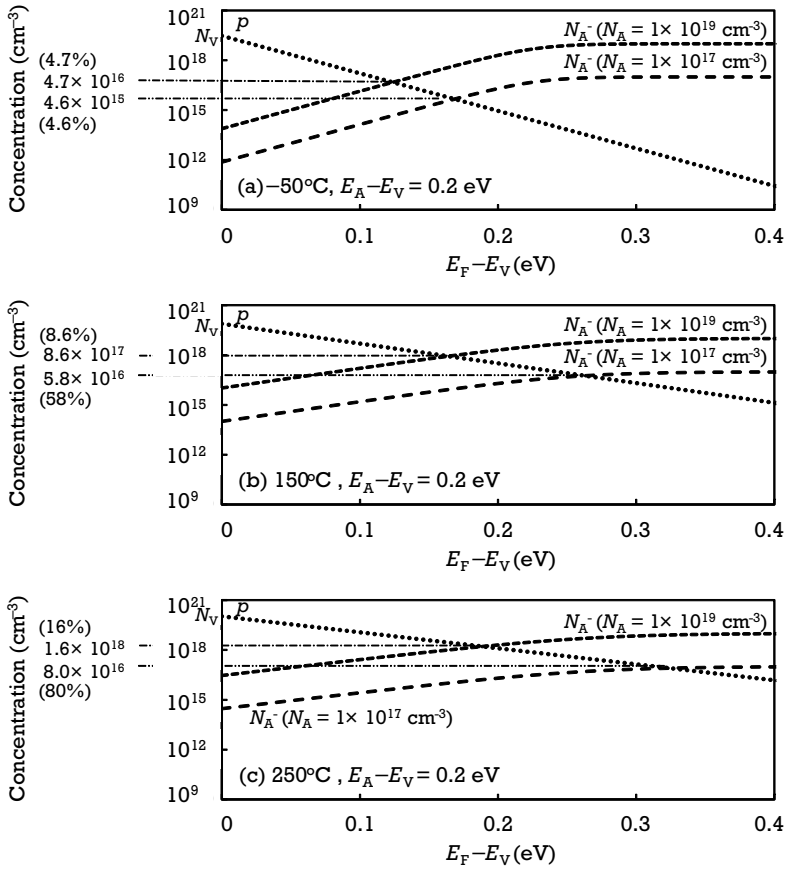

Figure 2.15 Shockley diagram to determine Fermi level E_F and hole concentration p in p-type GaN with acceptor ionization energy of 0.2 eV at (a) –50°C, (b) 150°C, and (c) 250°C. Each diagram shows two values of acceptor concentration, N_A.

where μ_n is called electron mobility. Since analogous arguments apply to holes, total drift current density J_{drift} can be written as

$$J_{drift} = (-q)n(-\mu_n E) + qp\mu_p E = q(n\mu_n + p\mu_p)E \tag{2.16}$$

Room-temperature μ_n and μ_p perpendicular to the c-axis are plotted in Figure 2.16 as a function of dopant density in GaN and 4H-SiC. Note that the μ_n values in the case of GaN and 4H-SiC are much larger than the μ_p value in the case of GaN and 4H-SiC. For that reason, electrons are chosen as carriers in low-on-resistance unipolar GaN and 4H-SiC power devices (see Chapters 8 and 9).

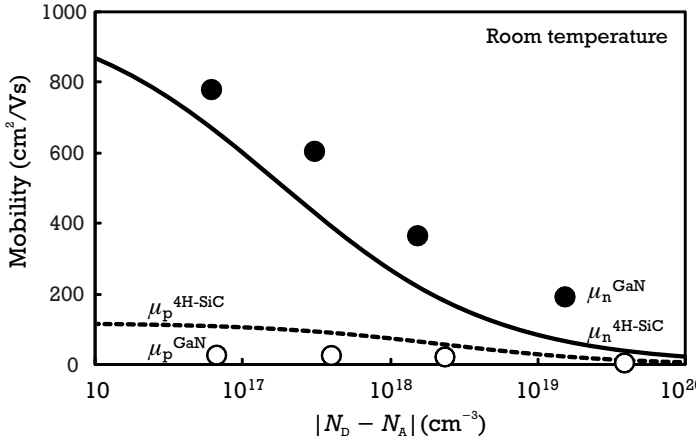

Figure 2.16 Room-temperature electron and hole mobility perpendicular to the *c*-axis in GaN [55, 58] and 4H-SiC [59, 60].

With respect to the reported μ_n at $N_D = 1 \times 10^{16}$ cm^{-3}, in the case of 6H-SiC, μ_n parallel to the *c*-axis was 60 cm^2/Vs, and μ_n perpendicular to the *c*-axis was 400 cm^2/Vs; in contrast, in the case of 4H-SiC, μ_n parallel to the *c*-axis was 900 cm^2/Vs, and μ_n perpendicular to the *c*-axis of 800 cm^2/Vs [61]. Such relatively isotropic electron transport is the reason 4H-SiC is preferred to 6H-SiC as a material for power devices.

2.6 Impact Ionization

Impact ionization is a process by which electron-hole pairs generated by carriers (mainly holes in the case of GaN [62] and 4H-SiC [63]) gain enough energy from an electric field (Figure 2.17). This process creates the onset of avalanche breakdown and is characterized by the impact-ionization coefficient, which is defined as the number of electron-hole pairs created by a mobile carrier traversing a unit length through the depletion region in the direction of the electric field. Although a lot of impact-ionization coefficients have been experimentally determined [62–68], they differ appreciably. This difference is probably due to the presence of defect, a nonuniform electric field, and the onset of premature breakdown at chip edges [62]. In this book, the largest critical electric field ($E_{critical}$) ever reported (i.e., 3.75 MV/cm [69] for GaN and 2.50 MV/cm for 4H-SiC [68]) is thus used instead of impact-ionization coefficients. Accordingly, avalanche breakdown can be assumed to occur simply when the maximum electric field equals to $E_{critical}$, whose slight dependence on T and N_D, for example, in the case of 4H-SiC [68],

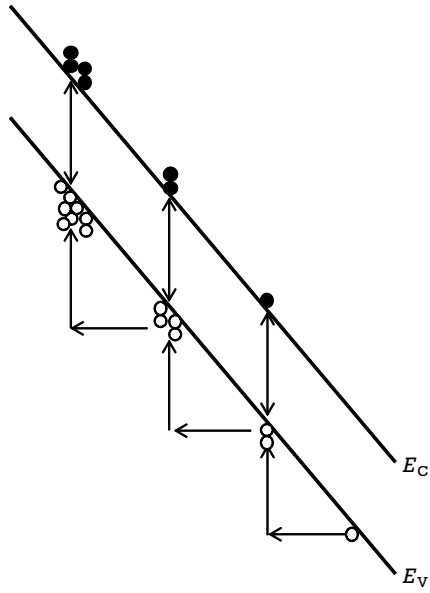

Figure 2.17 Multiplication of electrons and holes from impact ionization due to holes.

$$E_{\text{critical}} = (2.653 + 2.222 \times 10^{-6}\, T^2 - 1.166 \times 10^{-3} T)/[1–0.25 \log_{10}(N_D/10^{16})] \text{ MV/cm} \quad (2.17)$$

is ignored hereafter.

2.7 Figure of Merit

As a final section of this chapter on physical properties, Baliga's figure of merit for power devices (BFOM) [70] and Baliga's figure of merit for devices operating at high frequencies (BHFFOM) [71] are derived by considering a uniformly doped drift layer for unipolar power devices with a parallel-plane configuration. Poisson's equation is given as

$$dE(x)/dx = qN_D/\varepsilon_r\varepsilon_o \quad (2.18)$$

where ε_r is relative permittivity (i.e., 10.4 parallel to the *c*-axis of GaN [72] and 10.0 parallel to the *c*-axis of 6H-SiC [73]), and ε_o is permittivity in vacuum (i.e., 8.85×10^{-14} F/cm). As shown in Figure 2.18, the solution to (2.18) gives a triangular electric-field distribution. At the onset of avalanche breakdown, $E(0)$ can be assumed to be E_{critical}. Since the minimum thickness of the drift layer at which E becomes zero is W_D, N_D is given by

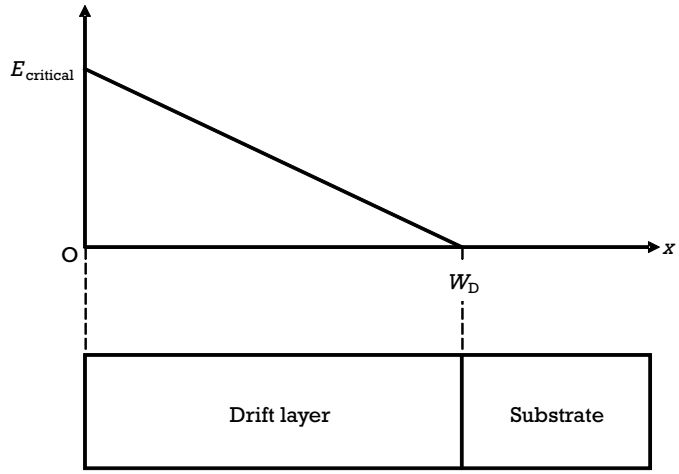

Figure 2.18 Uniformly doped drift layer and its electric-field distribution.

$$N_D = (\varepsilon_r \varepsilon_o / qW_D) E_{critical} \tag{2.19}$$

Breakdown voltage BV is equal to the area of the triangle, (i.e., $E_{critical}$ W_D /2), so W_D is given by

$$W_D = 2BV/E_{critical} \tag{2.20}$$

Since in an n-type drift layer, J_{drift} can be approximated from (2.16) as

$$J_{drift} \approx qN_D \mu_n (BV/W_D) \tag{2.21}$$

specific resistance of the ideal drift layer is obtained from (2.19)–(2.21) as

$$R_{ideal} = 4BV^2/\text{BFOM} \tag{2.22}$$

where

$$\text{BFOM} = \varepsilon_r \varepsilon_o \mu_n E_{critical}{}^3 \tag{2.23}$$

In the case of metal-insulator-semiconductor field-effect transistors (see Section 9.7) whose gate is biased at V_G, input capacitance per unit area C_I (see Section 9.2.2) is given as [71]

$$C_I = (\varepsilon_r \varepsilon_o q N_D / 2V_G)^{0.5} \tag{2.24}$$

By using (2.19) and (2.20) in (2.24), it can be shown that

$$C_I = \varepsilon_r \varepsilon_0 E_{critical}/2(V_G BV)^{0.5} \quad (2.25)$$

BHFFOM, which has the dimensions of frequency, is defined as [71]

$$\text{BHFFOM} = 1/R_{ideal} C_I \quad (2.26)$$

By using (2.22)–(2.24), (2.26) can be derived in terms of material parameters as follows:

$$\text{BHFFOM} = \mu_n E_{critical}^2 V_G^{0.5}/2BV^{1.5} \quad (2.27)$$

While ε_r and μ_n of GaN and 4H-SiC are comparable to those of silicon (i.e., 11.7 [74] and 1,000 cm^2/Vs [75]), $E_{critical}$ of GaN and 4H-SiC is about 10 times higher than $E_{critical}$ of silicon (i.e., 0.2 MV/cm [75]). As listed in Figure 2.19, calculated BFOM and BHFFOM of GaN and 4H-SiC are, respectively, more than 1,000 times and more than 100 times higher than those of silicon.

2.8 Summary

This chapter introduces the development history and physical properties of GaN and SiC with an emphasis on crystal structures. The chapter's description of crystal defects, especially stacking faults in 4H-SiC, will be referred to in Section 12.6. The chapter also briefly describes energy bands and impurity doping. To introduce the BFOM and BHFFOM, the chapter compares the relative permittivity, electron mobility, and critical-electric field in the case of GaN and 4H-SiC. On the basis of these described properties, this book compares vertical GaN and 4H-SiC power devices.

Semiconductor	$E_{critical}$	ε_r	μ_n	BFOM	BHFFOM
Si	1	1	1	1	1
GaN	19	0.9	0.9	5300	320
4H-SiC	13	0.9	0.9	1500	140

Figure 2.19 Material properties and calculated BFOM and BHFFOM.

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CHAPTER

3

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p-n Junctions

3.1 Introduction

To understand not only bipolar power devices (Chapter 10) but also edge terminations (Chapter 11), p-n junctions are of great importance. This chapter begins by introducing equations for the diffusion current. Subsequently, the chapter derives continuity equations and compares the carrier recombination lifetimes of GaN, 4H-SiC, and silicon. The basic theory of current/voltage characteristics developed by Shockley [1] is then explained. In addition, the chapter discusses the multidimensional effect on current/voltage characteristics of a non-self-aligned mesa-type p-n junction.

GaN and 4H-SiC power devices are often made from n-type starting material because their electron mobilities are higher than their hole mobilities (see Section 2.5). Therefore, this chapter mainly considers n-type GaN and 4H-SiC, as well as their junctions with heavily doped p-type (p^+) GaN and 4H-SiC.

3.2 Diffusion

When carrier concentration has a gradient, the carriers migrate from the high-concentration region to the low-concentration region by a process called diffusion. One-dimensional diffusion-current densities for electrons and holes are expressed, respectively, by Fick's law [2] as

$$J_{\text{n_diffusion}} = qD_{\text{n}}(\partial n/\partial x) \tag{3.1a}$$

and

$$J_{\text{p_diffusion}} = -qD_{\text{p}}(\partial p/\partial x), \tag{3.1b}$$

where D_{n} and D_{p} are diffusivity of electrons and holes, respectively. In an n-type semiconductor that is neither heavily doped (i.e., nondegenerate) nor under an external applied field, drift-current density of electrons (given by [2.16] as $qn\mu_{\text{n}}E$) balances $J_{\text{n_diffusion}}$ as follows:

$$qn\mu_{\text{n}}E + qD_{\text{n}}(\partial n/\partial x) = 0 \tag{3.2}$$

Under the thermal equilibrium condition, the Fermi level E_{F} must be constant. Therefore, the partial derivative of electron concentration $n = N_{\text{C}} \exp[-(E_{\text{C}}-E_{\text{F}})/kT]$ (see [2.12a]) with respect to x becomes

$$\partial n/\partial x = -(N_{\text{C}}/kT)\ (\partial E_{\text{C}}/\partial x)\ \exp[-(E_{\text{C}}-E_{\text{F}})/kT] \tag{3.3}$$

Since

$$qE = \partial E_{\text{C}}/\partial x \tag{3.4}$$

(3.3) becomes

$$\partial n/\partial x = -qEn/kT \tag{3.5}$$

Combining (3.2) and (3.5) gives the following Einstein relation for an n-type semiconductor

$$D_{\text{n}} = (kT/q)\ \mu_{\text{n}} \tag{3.6a}$$

Similarly, for a nondegenerate p-type semiconductor, the Einstein relation becomes

$$D_{\text{p}} = (kT/q)\ \mu_{\text{p}} \tag{3.6b}$$

3.3 Continuity Equations

An infinitesimal slice of a crystal (thickness: dx; cross-sectional area: A) located at x is treated one-dimensionally (Figure 3.1). The number of electrons flowing into the slice and flowing out of the slice are, respectively, $J_n(x)/(-q)$ and $J_n(x+dx)/(-q)$. When the generation and recombination rates per unit volume for electrons are represented, respectively, by G_n and R_n, the rate of change in the number of electrons in the slice is given by

$$(\partial n/\partial t)Adx = [J_n(x)/(-q) - J_n(x+dx)/(-q)]A + (G_n - R_n)A\,dx \tag{3.7}$$

Expanding the second term on the right-hand side in a Taylor series gives the following continuity equation:

$$\partial n/\partial t = (1/q)(\partial J_n(x)/\partial x) + (G_n - R_n) \tag{3.8a}$$

For holes, the continuity equation (3.8b) is similarly obtained; as suggested the sign of $(-q)$ on the right-hand side of (3.8a) is switched.

$$\partial p/\partial t = (-1/q)\ (\partial J_p(x)/\partial x) + (G_p - R_p) \tag{3.8b}$$

According to (2.16) (namely, $J_{drift} = q(n\mu_n + p\mu_p)E$), electron and hole drift-current densities are given as

$$J_{n_drift} = qn\mu_n E \tag{3.9a}$$

and

$$J_{p_drift} = qp\mu_p E \tag{3.9b}$$

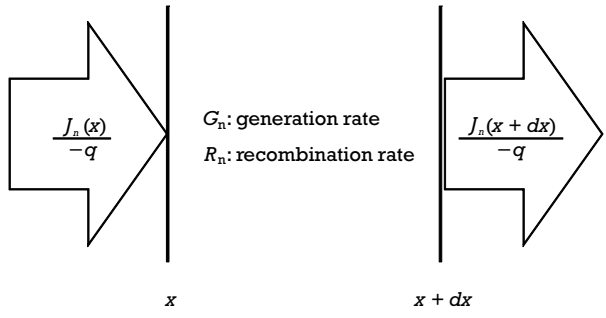

Figure 3.1 Increase in electron concentration in an infinitesimal slice (thickness: dx; cross-sectional area: A) related to net flow of electrons into the slice and excess of generation over recombination.

Combining (3.9a, b) with (3.1a, b), respectively, gives the following equations of total current densities of electrons and holes:

$$J_n = qn\mu_n E + qD_n(\partial n/\partial x) \tag{3.10a}$$

and

$$J_p = qp\mu_p E - qD_p(\partial p/\partial x) \tag{3.10b}$$

Inserting (3.10a, b), respectively, into (3.8a, b) and assuming that mobilities and diffusivities are independent of x gives the final form of continuity equations for electrons and holes, respectively, as

$$\partial n/\partial t = \mu_n n(x)(\partial E/\partial x) + \mu_n E(x)(\partial n/\partial x) + D_n \partial^2 n/\partial x^2 + (G_n - R_n) \tag{3.11a}$$

and

$$\partial p/\partial t = -\mu_p p(x)(\partial E/\partial x) - \mu_p E(x)(\partial p/\partial x) + D_p \partial^2 p/\partial x^2 + (G_p - R_p). \tag{3.11b}$$

3.4 Carrier Recombination Lifetime

An external stimulus, such as photonic or thermal energy, creates excess carriers. When the external stimulus is removed, the excess carrier concentration decays to the equilibrium value mainly through (1) band-to-band (Figure 3.2[a]) (2) Shockley-Read-Hall (SRH) (Figure 3.2[b]), and (3) Auger (Figure 3.2[c]) recombination processes.

3.4.1 Band-to-Band Recombination Lifetime

The band-to-band recombination rate $R_{\text{band-to-band}}$ is proportional to electron and hole concentrations, namely

$$R_{\text{band-to-band}} = Bnp, \tag{3.12}$$

where B is the band-to-band recombination coefficient (i.e., 1.2×10^{-11} cm^3/s for GaN [3], 1.5×10^{-12} cm^3/s for 4H-SiC [4], and 4.7×10^{-15} cm^3/s for Si [5]). The relatively large B for GaN is attributed to the direct bandgap (see Section 2.3). Note that even among the indirect semiconductors, B for

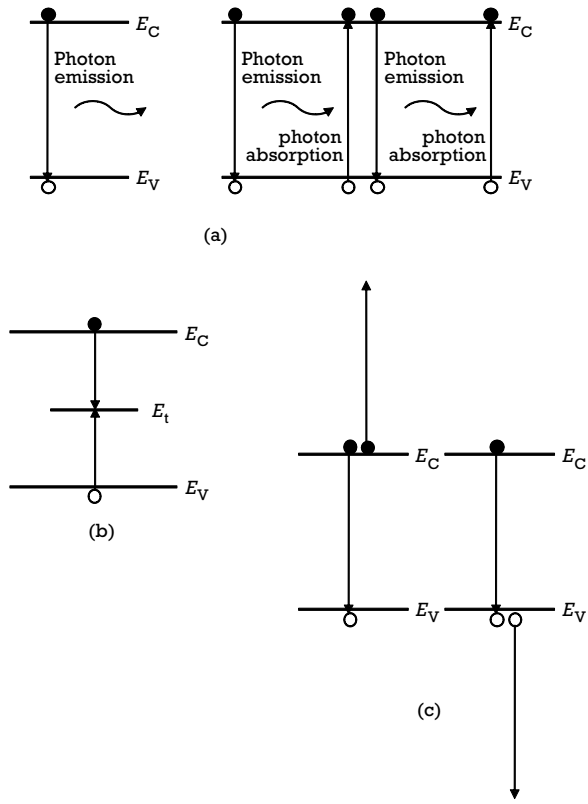

Figure 3.2 Schematic illustration of (a) band-to-band recombination, (b) Shockley-Read-Hall recombination, and (c) Auger recombination. Band-to-band recombination with reabsorption of recombination radiation (i.e., photon recycling) is also shown in (a).

4H-SiC is more than 300 times larger than B for Si. This considerable difference in B is quantitatively discussed in Section 3.4.4.

Band-to-band recombination plays an important role in determining carrier lifetimes under high-level injection (i.e., when excess-carrier concentration p [= n, due to charge neutrality] is larger than the majority-carrier concentration). Electron and hole concentrations in an n-type semiconductor under high-level injection are given, respectively, as

$$n_n = N_D + p \approx p \tag{3.13a}$$

and

$$p_n = p_{no} + p \approx p \tag{3.13b}$$

where p_{no} is hole concentration under thermal equilibrium.

$R_{\text{band-to-band}}$ in an n-type semiconductor under high-level injection is thus given as

$$R_{\text{band-to-band_p}} = B\Delta p^2 \equiv \Delta p/\tau_{\text{band-to-band_p}} \tag{3.14a}$$

where the band-to-band recombination lifetime under high-level injection is

$$\tau_{\text{band-to-band_p}} = 1/(B\Delta p) \tag{3.14b}$$

As described in Section 2.3, the optical-absorption coefficient of GaN is much larger than that of 4H-SiC. In the case of GaN, radiative recombination is therefore often reabsorbed (i.e., photon recycling) (Figure 3.2[a]), effectively increasing $\tau_{\text{band-to-band_p}}$, namely, decreasing B. Photon recycling is described in detail in Chapter 4.

3.4.2 SRH Recombination Lifetime

In any semiconductor, localized states in an energy gap (Figure 3.2[b]), due to such factors as point defects (Section 2.2.3) and impurity atoms, are practically present. According to analyses by Shockley and Read [6] and Hall [7], the recombination rate U_{SRH} in the steady state via a single deep-level recombination center is given as

$$\begin{aligned} U_{\text{SRH}} &= \sigma_n\sigma_p v_{\text{th}} N_t (np - n_i^2)/[\sigma_n(n + n_1) + \sigma_p(p + p_1)] \\ &= (np - n_i^2)/[(n + n_1)/(\sigma_p v_{\text{th}} N_t) + (p + p_1)/(\sigma_n v_{\text{th}} N_t)] \end{aligned} \tag{3.15}$$

where σ_n and σ_p are, respectively, capture cross-sections for electrons and holes, v_{th} is thermal velocity, N_t is trap concentration, and n_1 and p_1 are, respectively, equilibrium electron and hole concentrations when E_F coincides with trap level E_t. Namely,

$$n_1 = n_i \exp[(E_t - E_i)/kT] \tag{3.16a}$$

and

$$p_1 = n_i \exp[(E_i - E_t)/kT], \tag{3.16b}$$

where E_i is the intrinsic Fermi level (i.e., the mid-gap level). Since the minority-carrier lifetimes in heavily doped p-type and n-type semiconductors are respectively defined as

$$\tau_{p0} = 1/(\sigma_p v_{th} N_t) \tag{3.17a}$$

and

$$\tau_{n0} = 1/(\sigma_n v_{th} N_t), \tag{3.17b}$$

(3.15) can be expressed as

$$U_{SRH} = (np - n_i^2)/[\tau_{p0}(n+n_1)+\tau_{n0}(p+p_1)] \tag{3.18}$$

The dependence of U_{SRH} on E_t in (3.18) can be expressed by assuming $\sigma_n = \sigma_p \equiv \sigma_0$ and $\tau_{n0} = \tau_{p0} \equiv \tau_0$ as follows:

$$U_{SRH} = (np - n_i^2)/\{n+p+2n_i \cosh[(E_t - E_i)/kT]\tau_0\} \tag{3.19}$$

Here, it is considered that an n-type semiconductor with no current flow is disturbed by creation of equal numbers of excess electrons and holes. If low-level injection is considered, Δn and Δp are much less than (n_0+p_0), where n_0 and p_0 denote, respectively, thermal-equilibrium electron and hole concentrations. The continuity equation for excess holes (3.11b) becomes

$$\begin{aligned} \partial \Delta p/\partial t &= G_p - R_p = -U_{SRH} \\ &= [-(n_0 + p_0)\Delta p]/\{n_0 + p_0 + 2n_i \cosh[(E_t - E_i)/kT]\tau_0\} \end{aligned} \tag{3.20}$$

For recombination centers around the mid-gap level, $(E_t - E_i)$ becomes negligibly small, so (3.20) can be expressed as

$$\partial \Delta p/\partial t \equiv -\Delta p/\tau_{SRH_p} \tag{3.21a}$$

and

$$\tau_{SRH_p} = \tau_0 = \tau_{p0} = 1/(\sigma_p v_{th} N_t) \tag{3.21b}$$

Equation (3.21b) indicates that the SRH lifetime of holes in an n-type semiconductor (τ_{SRH_p}) is independent of majority-carrier concentration N_D under low-level injection.

3.4.3 Auger Recombination Lifetime

When excess carriers recombine in a region with a large dopant concentration, the probability of direct recombination between electrons

and holes (Figure 3.2[c]) may not be neglected. In such a recombination process (called Auger recombination), three free carriers interact; namely, either two electrons and a hole or two holes and an electron (Figure 3.2[c]). The Auger recombination rate U_A is given as

$$U_A = C_n n(np - n_i^2) + C_p p(np - n_i^2) \tag{3.22}$$

where C_n and C_p are coefficients for interactions in which the remaining carrier is an electron or a hole, respectively. In the case of Auger recombination in an n-type semiconductor, if $C_n \approx C_p$, the second term on the right-hand side of (3.22) is smaller than the first term on the right-hand side of (3.22). The Auger-recombination lifetime of excess holes Δp is thus given as

$$\tau_{A_p} = \Delta p / U_A \approx 1/(C_n N_D^2) \tag{3.23}$$

Reported C_n values are about the same for GaN (4.5×10^{-31} cm^6/s [8]), 4H-SiC (5.0×10^{-31} cm^6/s for [9]), and Si (2.8×10^{-31} cm^6/s [10]).

3.4.4 Overall Expression for Carrier Recombination Lifetime

If the dependence of τ_{SRH_p} on Δp is neglected, an overall expression for the recombination lifetime of holes in an n-type semiconductor is given as

$$\tau_p = 1/[(1/\tau_{band\text{-}to\text{-}band_p}) + (1/\tau_{SRH_p}) + (1/\tau_{A_p})] \tag{3.24}$$

The values of B and C_n described in Sections 3.4.1 and 3.4.3 are used to calculate τ_p, which was calculated as a function of Δp when $N_D = 1 \times 10^{14}$ cm^{-3} (Figure 3.3). In the case of silicon, Auger recombination limits τ_p under high-level injection when τ_{SRH_p} exceeds 10 μs (Figure 3.3[a]). In the case of 4H-SiC, on the other hand, band-to-band recombination limits τ_π under high-level injection when τ_{SRH_p} exceeds 1 μs (Figure 3.3[b]). The latter result is mainly due to the relatively large B for 4H-SiC.

In the case of GaN, if the effect of photon recycling is not present, τ_p reduces to about 10% of τ_p for 4H-SiC at a fixed excess-carrier concentration. This is because band-to-band recombination limits τ_p even when τ_{SRH_p} is 100 ns (Figure 3.3[c]). However, the dependence of τ_p on excess-carrier concentration for GaN under the effect of photon recycling is comparable to that for 4H-SiC for the following reason. For example, in the case of AlGaAs/GaAs heterostructures, photon recycling factor Φ (i.e., effective band-to-band recombination lifetime $\tau_{band\text{-}to\text{-}band}^{eff}$ divided by $\tau_{band\text{-}to\text{-}band_p}$) of 4–6 was reported [11]. In Figure 3.3(d), Φ of 8 is assumed simply because $\tau_{band\text{-}to\text{-}band}^{eff}$ for GaN becomes equal to $\tau_{band\text{-}to\text{-}band_p}$ for 4H-SiC. Since C_n for

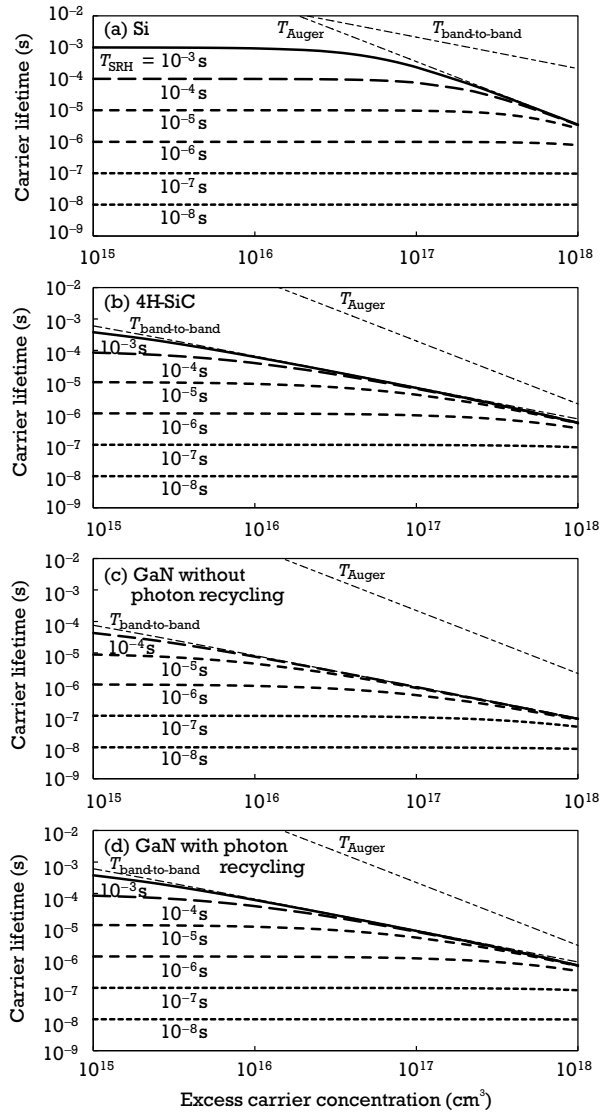

Figure 3.3 Calculated recombination lifetime in the case of n-type (a) silicon, (b) 4H-SiC, (c) GaN without photon recycling, and (d) GaN with photon recycling (photon recycling factor: 8) as a function of excess-carrier concentration. Band-to-band and Auger recombination coefficients used are, respectively, 4.7×10^{-15} cm^3/s and 2.8×10^{-31} cm^6/s for silicon, 1.5×10^{-12} cm^3/s and 5.0×10^{-31} cm^6/s for 4H-SiC, and 1.2×10^{-11} cm^3/s and 4.5×10^{-31} cm^6/s for GaN.

GaN is about the same as that for 4H-SiC (see Section 3.4.3), the dependences of τ_p on excess-carrier concentration are similar in the case of GaN and 4H-SiC.

3.5 Depletion-Region Width of One-Dimensional p^+n Abrupt Junction

The following depletion approximation, which assumes box-profile depleted charges with width W_{Dp} in the p^+region and W_{Dn} in the n-region, is used for simple analysis (Figure 3.4[a]). Since the electric field in the neutral regions is almost zero, the following equation must be satisfied:

$$N_A W_{Dp} = N_D W_{Dn} \tag{3.25}$$

Since the Poisson equation is expressed as

$$\partial E/\partial x = -qN_A/\varepsilon_r\varepsilon_o \text{ for } -W_{Dp} \le x \le 0 \tag{3.26a}$$

and

$$\partial E/\partial x = qN_D/\varepsilon_r\varepsilon_o \text{ for } 0 \le x \le W_{Dn} \tag{3.26b}$$

the electric field is obtained by integrating (3.26a, b) as follows:

$$E(x) = -qN_A(x+W_{Dp})/\varepsilon_r\varepsilon_o \text{ for } -W_{Dp} \le x \le 0 \tag{3.27a}$$

and

$$E(x) = -E_{max}+qN_D x/\varepsilon_r\varepsilon_o = -qN_D(W_{Dn}-x)/\varepsilon_r\varepsilon_o \text{ for } 0 \le x \le W_{Dn} \tag{3.27b}$$

where E_{max} is the maximum electric field (Figure 3.4[b]) expressed as

$$E_{max} = qN_A W_{Dp}/\varepsilon_r\varepsilon_o = qN_D W_{Dn}/\varepsilon_r\varepsilon_o \tag{3.28}$$

As shown in Figure 3.4(b, c), the total depletion-region width W_D and built-in potential Ψ_{bi} can be approximated, respectively, by W_{Dn} and Ψ_n because W_{Dp} and Ψ_p are much smaller than W_{Dn} and Ψ_n in the case of a p^+n abrupt junction. Integrating (3.27b) gives Ψ_{bi} as

$$\Psi_{bi} \approx qN_D W_{Dn}^2/2\varepsilon_r\varepsilon_o \tag{3.29}$$

From (3.29), W_D of a one-dimensional p^+n abrupt junction is expressed as

$$W_D \approx (2\varepsilon_r\varepsilon_o\Psi_{bi}/qN_D)^{0.5} \tag{3.30}$$

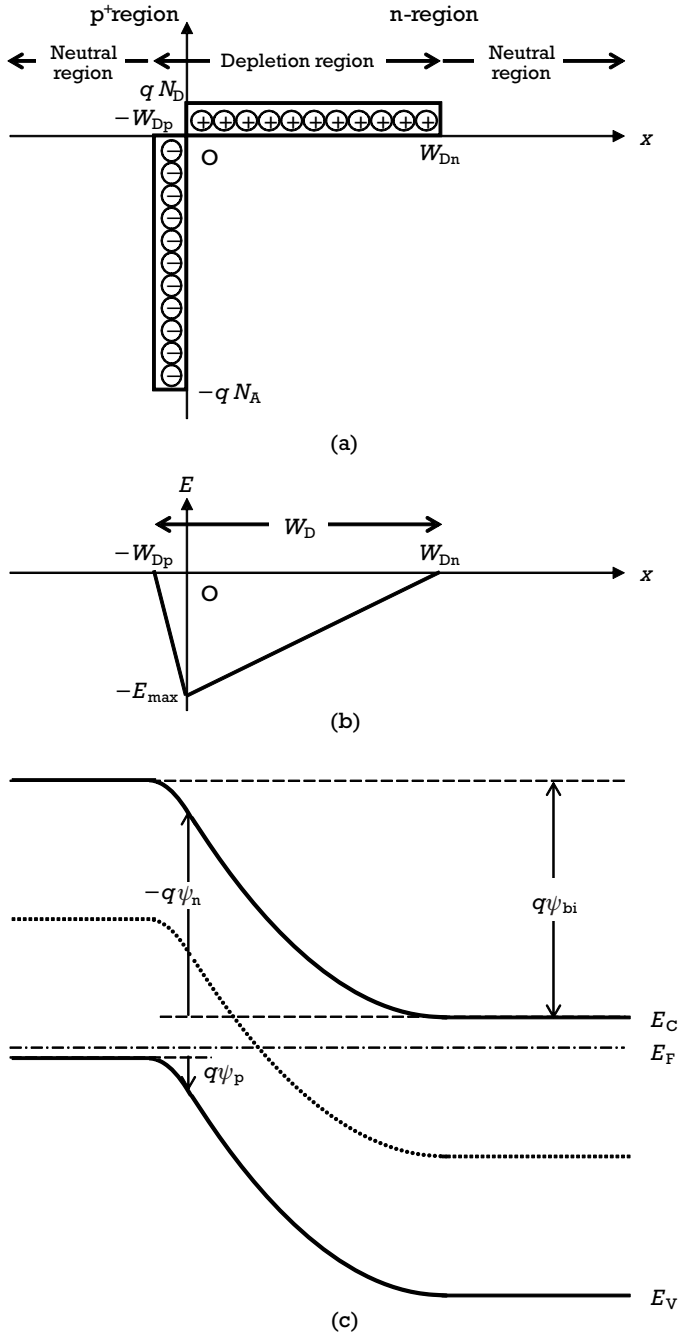

Figure 3.4 Abrupt p^+n junction under thermal equilibrium: (a) space-charge distribution under depletion approximation, (b) electric-field distribution, and (c) energy-band diagram.

3.6 One-Dimensional Forward-Current/Voltage Characteristics

A one-dimensional p^+n junction is considered to be connected to a voltage source with the n-region grounded and the p^+region at V volts relative to ground. The junction is assumed to be not illuminated, so carrier concentration is only influenced by V. Furthermore, ohmic drops are assumed to be neglected, so V is sustained entirely at the junction; that is, total junction voltage is $\Psi_{bi}-V$.

3.6.1 Low-Level Injection Condition

Electron concentration at the quasi-neutral boundary in the n-region next to the p^+n junction (i.e., $x = W_{Dn} \approx W_D$) can be assumed to be equal to N_D regardless of whether the junction is at equilibrium or under bias. Here, W_D under bias is given by (3.30) by replacing Ψ_{bi} with $\Psi_{bi}-V$ to give

$$W_D \approx [2\varepsilon_r\varepsilon_o(\Psi_{bi}-V)/qN_D]^{0.5} \tag{3.31}$$

If hole concentration in the p^+region under thermal equilibrium is denoted as p_{p0}, $p(W_D)$ under low-level injection is approximated by

$$p(W_D) \approx p_{p0} \exp[-q(\Psi_{bi}-V)/kT] = (n_i^2/N_D^+) \exp(qV/kT) \tag{3.32}$$

3.6.1.1 Diffusion Current

The continuity equation (3.11b) for the neutral n-region under steady state is given as

$$0 = D_p\partial^2\Delta p/\partial x^2 - \Delta p(x)/\tau_{SRH_p} \tag{3.33}$$

Equation (3.33) has the simple exponential solution

$$\Delta p(x) = A \exp[-(x-W_D)/(D_p\tau_{SRH_p})^{0.5}] + B \exp[(x-W_D)/(D_p\,\tau_{SRH_p})^{0.5}] \tag{3.34}$$

where constants A and B are determined by boundary conditions. If neutral n-region width is much larger than diffusion length $L_p \equiv (D_p\,\tau_{SRH_p})^{0.5}$, L_p represents the average distance traveled in the neutral n-region before a hole injected from the p^+region recombines. Since $\Delta p(x)$ must decrease with increasing x, B in (3.34) must be zero. By combining (3.32) and (3.34), it follows that

$$\Delta p(x) = (n_i^2/N_D^+) \left[\exp(qV/kT)-1\right] \exp[-(x-W_D)/L_p] \tag{3.35}$$

Since hole current flows only by diffusion at $x = W_D$ (Figure 3.5[a]), total current density flowing through the p^+n junction is given as

$$J_{total} = Jp(x)|_{x=W_D} = -qD_p \partial \Delta p / \partial x|_{x=W_D} = J_S^{LL}\left[\exp(qV/kT)-1\right] \tag{3.36a}$$

and

$$J_S^{LL} = qD_p n_i^2/(N_D^+ L_p) \tag{3.36b}$$

In the case that N_A^- in the p^+region is decreased (Figure 3.5[b]), J_{total} can be expressed as the sum of $J_{p_diffusion}(W_{Dn})$ and $J_{n_diffusion}(-W_{Dp})$. By combining (3.35) and (3.36a, b), J_{total} can be expressed as

$$J_{total} = qn_i^2 \left[D_p/(N_D^+ L_p)+D_n/(N_A^- L_n)\right] \left[\exp(qV/kT)-1\right] \tag{3.37}$$

In the case that the thickness of the p-region (W_p) is less than L_n (Figure 3.5[c]), the expression for $J_{n_diffusion}(-W_{Dp})$ changes to

$$J_{n_diffusion}\left(-W_{D_p}\right) = qn_i^2 D_n / \left(N_A - W_p\right)\left[\exp\left(qV/kT\right)-1\right] \tag{3.38}$$

J_{total} therefore becomes

$$J_{total} = qn_i^2 \left[D_p/(N_D^+ L_p)+D_n/(N_A - W_p)\right] \left[\exp(qV/kT)-1\right] \tag{3.39}$$

When the diode current density is proportional to $[\exp(qV/nkT)-1]$, n is called the ideality factor. Equations (3.36a), (3.37), and (3.39) show that the ideal diffusion current under low-level injection has an ideality factor of unity.

3.6.1.2 Space-Charge Recombination Current

In addition to J_{total} expressed by (3.36a), (3.37), and (3.39), space-charge recombination current density $J_{recombination}$ also exits. $J_{recombination}$ is also important because it becomes larger than J_{total} when V is small. From the mass-action law and (3.32), it follows that

$$n\,p = n_i^2 \exp(qV/kT) \tag{3.40}$$

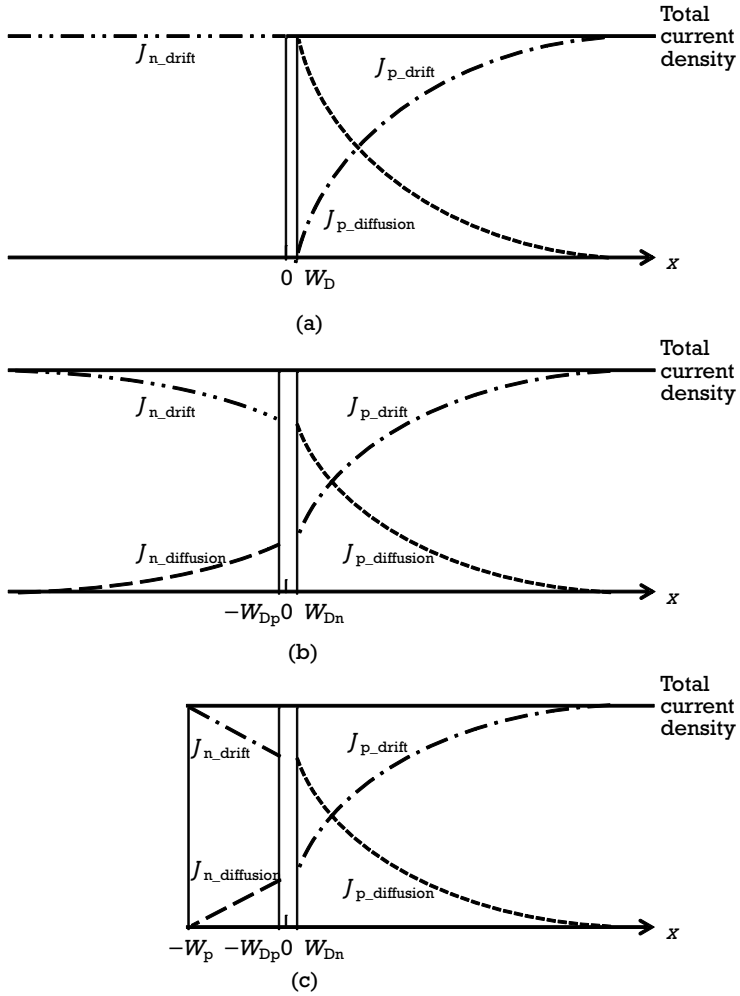

Figure 3.5 Current-density components under low-level injection around (a) thick p^+n, (b) thick p-n, and (c) thin p-n abrupt junctions.

Inserting (3.40) into (3.19) gives

$$U_{SRH} = n_i^2\,[\exp(qV/kT)-1]/\{n+p+2n_i\cosh[(E_t-E_i)/kT]\tau_0\}$$
$$\approx n_i^2\exp(qV/kT)/\{n+p+2n_i\cosh[(E_t-E_i)/kT]\tau_0\} \quad (3.41)$$

Since the denominator of (3.41) reaches a minimum when $n = p$ and $E_t = E_i$, maximum U_{SRH} is given as

$$U_{SRH}{}^{max} \approx (n_i/2\tau_0)\exp(qV/2kT) \quad (3.42)$$

Under the assumption that most of the depletion layer has ${U_{\mathrm{SRH}}}^{\max}$, maximum $J_{\mathrm{recombination}}$ can be approximated as

$$\begin{aligned} {J_{\mathrm{recombination}}}^{\max} &\approx q{U_{\mathrm{SRH}}}^{\max}W_{\mathrm{D}} \\ &= {J_{\mathrm{S}}}^{\mathrm{R}} \exp(qV/2kT) \end{aligned} \tag{3.43a}$$

and

$${J_{\mathrm{S}}}^{\mathrm{R}} = qW_{\mathrm{D}}n_{\mathrm{i}}/2\tau_0 \tag{3.43b}$$

Equation (3.43a) shows that the space-charge recombination current under low-level injection has an ideality factor of two.

3.6.2 High-Level Injection Condition

Even under high-level injection, charge neutrality can be assumed to hold at every point (i.e., $\partial\Delta p(x) \approx p(x)$ is equal to $\partial\Delta n(x) \approx n(x)$). Based on (3.32), in the case of W_{D} being larger than the drift-layer thickness $2d$,

$$p(2d) \approx n_{\mathrm{i}} \exp(qV/2kT) \tag{3.44}$$

is obtained. J_{total} then becomes roughly proportional to $\exp(qV/2kT)$, showing that the high-level injection current has an ideality factor of two. Its proportional constant is given by [12]

$$\begin{aligned} {J_{\mathrm{S}}}^{\mathrm{HL}} = \{&2qD_{\mathrm{a}}{N_{\mathrm{C}}}^{0.5}{N_{\mathrm{V}}}^{0.5} \tanh(d/L_{\mathrm{a}})/L_{\mathrm{a}}/[1-0.25\tanh^4(d/L_{\mathrm{a}})]^{0.5}\} \\ &\times \exp[-(E_{\mathrm{g}}+qV_{\mathrm{M}})/(2kT)] \end{aligned} \tag{3.45}$$

where V_{M} is the voltage drop across the drift layer, and D_{a} is ambipolar diffusivity defined as

$$D_{\mathrm{a}} = 2D_{\mathrm{n}}D_{\mathrm{p}}/(D_{\mathrm{n}}+D_{\mathrm{p}}) \tag{3.46}$$

and L_{a} is the ambipolar diffusion length defined as

$$L_{\mathrm{a}} = (D_{\mathrm{a}}\,\tau_{\mathrm{HL}})^{0.5} \tag{3.47}$$

where τ_{HL} is the high-level injection lifetime.

3.6.3 An Example of Measured Current/Voltage Characteristics

On the basis of the equations described in Sections 3.6.1 and 3.6.2, J_{total} is expressed as

$$J_{total} = J_S^{R}\exp(qV/2kT)+J_S^{LL}\exp(qV/kT)+J_S^{HL}\exp(qV/2kT) \quad (3.48)$$

where the effect of series resistance is neglected. An example of the measured current/voltage characteristics of a circular-mesa GaN p^+n diode with a diameter of 60 μm [13], together with the three extracted components on the right-hand side of (3.48) is shown in Figure 3.6. The layered structure of the diode consists of p^+GaN ($N_A = 2 \times 10^{19}$ cm^{-3} / 0.5 μm), n-GaN ($N_D = 2 \times 10^{16}$ cm^{-3} / 10 μm), and n^+GaN ($N_D = 2 \times 10^{18}$ cm^{-3} / 2 μm) on a GaN (0001) freestanding substrate [13]. In this example, space-charge recombination with $n = 2$ dominates the forward current when V is less than 2.8V. A current component of low-level injection with $n = 1$ is added in the V range from 2.8 to 2.9V. From 2.9 to 3.0V, on the other hand, the forward current is dominated by a current component of high-level injection with $n = 2$.

The measurement results plotted in Figure 3.6 deviate from the line representing the current component of high-level injection when V is greater than 3.0V. Such deviation has generally been attributed to a series-resistance

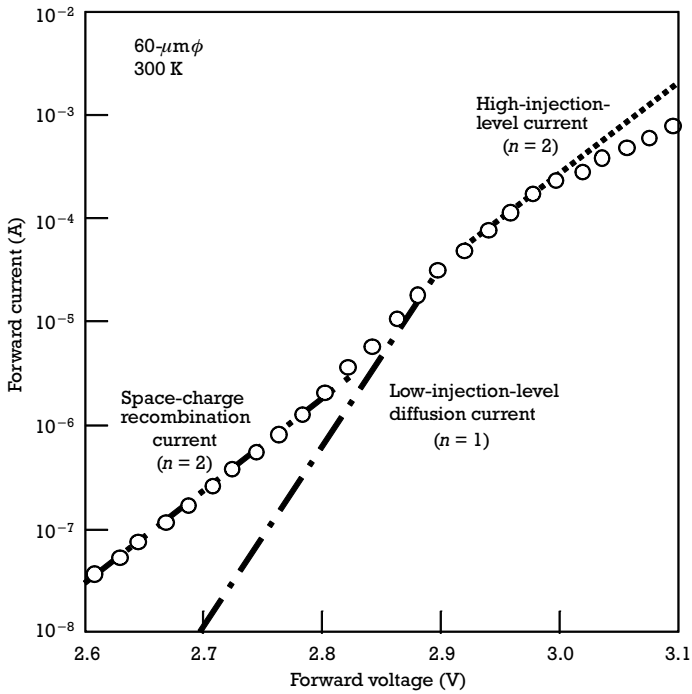

Figure 3.6 Example of measured forward current/voltage characteristics of a GaN p^+n diode (open circles [13]), together with the extracted current components: space-charge recombination with ideality factor n of two, low-level injection with $n = 1$, and high-level injection with $n = 2$.

effect [14]. In that V range, however, a multidimensional effect (described in Section 3.7) has to be taken into account.

3.7 Multidimensional Forward-Current/Voltage Characteristics

This section clarifies the multidimensional effects concerning a forward-biased p^+n junction. In the case of Si p^+n diodes, a planar structure, where a p^+region is formed by ion implantation and diffusion of acceptors, is usually adopted (Figure 3.7[a]). However, a planar structure is not suitable for either GaN or 4H-SiC p^+n diodes for the following reasons. Although magnesium can be implanted into GaN [15–17], the activation ratio of magnesium acceptors is very low, which results in a large ideality-factor (i.e., 2.6) and a low forward-current-density (i.e., 1 A/cm^2) of p-n diodes [17]. In the case of 4H-SiC, aluminum implantation has been frequently used; however, conductivity modulation has not been fully achieved with the use of ion implantation [18]. The use of ion implantation for active regions is thus avoided in the cases of GaN and 4H-SiC p^+n diodes.

The p^+region of GaN and 4H-SiC p^+n diodes is usually made of a p^+ epitaxial layer grown on an n-type epitaxial layer (Figure 3.7[b]). (The epitaxial growth is described in detail in Chapter 6.) To define the area of the active region, a mesa structure (Figure 3.7[c]) must therefore inevitably be formed. (Chapter 7 details device processing, including etching.) Fabrication of mesa-type p^+n diodes is finished with the formation of cathode and anode electrodes on the backside and top of the p^+n diodes, respectively. In such mesa-type p^+n diodes, especially small ones, peripheral current due to surface recombination increases. Furthermore, the anode electrode is usually formed with a non-self-aligned process, especially because annealing is required for activating magnesium acceptors in GaN [19, 20]. In such non-self-aligned mesa-type p^+n diodes, peripheral current due to electric-filed concentration also increases.

3.7.1 Influence of Surface Recombination on Peripheral Current of p^+n Diodes

3.7.1.1 Surface-Recombination Velocity

Section 3.4.2 discusses SRH recombination centers uniformly distributed in the bulk of a semiconductor material. Similarly, at a semiconductor surface, localized states (E_{st}) are located within the energy gap. Instead of the volume density of bulk centers, the area density of surface centers [N_{st} (cm^{-2})] is treated here. When $\sigma_n = \sigma_p \equiv \sigma$, (3.15) and (3.16a, b) reduce to

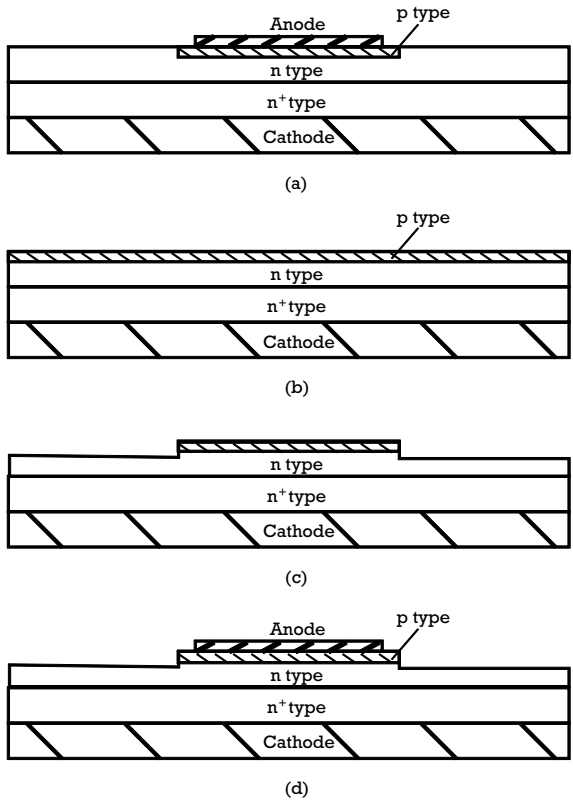

Figure 3.7 Schematic cross-sections of (a) planar and (d) mesa-type p^+n diodes: (b) and (c): show fabrication processes of mesa-type p^+n diodes.

$$U_s = \sigma\, v_{th}\, N_{st}\, (n_s\, p_s - n_i^2)\ /\ (n_s + n_{1s} + p_s + p_{1s}) \tag{3.49a}$$

$$n_{1s} = n_i \exp\, [(E_{st} - E_i)\ /\ k\, T] \tag{3.49b}$$

$$p_{1s} = n_i \exp\, [(E_i - E_{st})\ /\ k\, T] \tag{3.49c}$$

where n_s and p_s are, respectively, electron and hole concentrations near the surface. If product np is assumed to be constant throughout the surface space-charge region in an n-type semiconductor,

$$n_s\, p_s = N_D^+\, p' \tag{3.50}$$

where p' is hole concentration at the neutral edge of the space-charge region. When $E_{st} \approx E_i$, (3.49a) reduces to

$$U_s = \sigma\, v_{th}\, N_{st}\, N_D^+ \,[p' - (n_i^2 / N_D^+)] \,/\, (n_s + p_s + 2\, n_i)$$
$$= s\, \Delta\, p' \tag{3.51a}$$

$$s = \sigma\, v_{th}\, N_{st}\, N_D^+ \,/\, (n_s + p_s + 2\, n_i) \tag{3.51b}$$

where s is surface-recombination velocity, and $\Delta p'$ is excess-hole concentration at the neutral edge of the space-charge region. If the surface is neutral, $N_D^+/\,(n_s+p_s+2n_i)$ is unity, so s can be expressed as

$$s = \sigma v_{th} N_{st} \tag{3.52}$$

3.7.1.2 Simulation of the Influence of Surface Recombination

The current/voltage characteristics of the GaN p^+n diodes described in Section 3.6.3 were simulated in a cylindrical coordinate system (Figure 3.8) by using a commercial simulator [21]. The over-etched depth of the n-GaN drift layer was assumed to be 0.5 μm, and the simulation parameters used were the same as those reported in [13] and [22]. To identify the location where the surface recombination dominates the measured forward current, one of the following surface-recombination velocities was used as a parameter: s_1 on the side surface of p^+GaN; s_2 on the side surface of n-GaN; or s_3 on the surface of etched n-GaN.

As shown in Figure 3.9, the measured mesa-diameter dependence of the forward current at 2.7V is well reproduced with s_2 = 1×10^8 cm/s. The slope of unity also confirms that the current simulated with s_2 is a peripheral current. On the other hand, the dependences

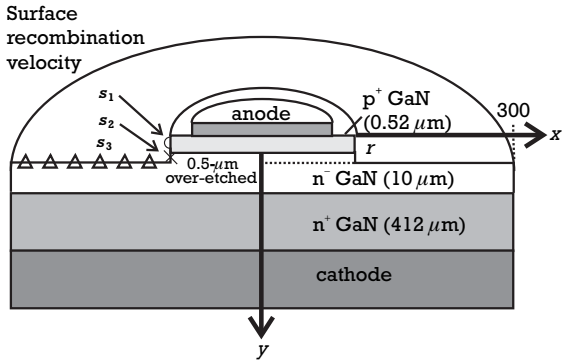

Figure 3.8 Schematic of a simulated GaN p^+n diode, including the following three surface-recombination velocities: s_1 on the side surface of p^+GaN; s_2 on the side surface of n-GaN; and s_3 on the surface of etched n-GaN.

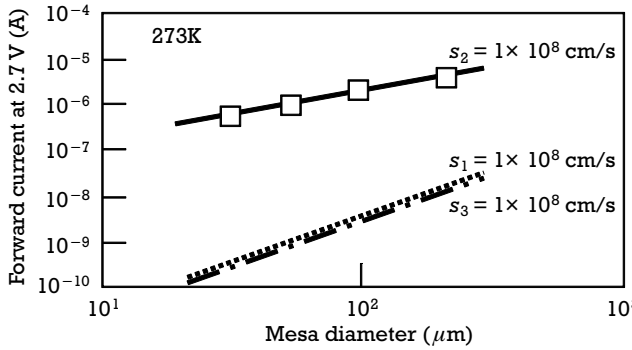

Figure 3.9 Measured (open squares [13]) and simulated 2.7-V forward-biased currents of GaN p$^+$n diodes as a function of mesa diameter.

simulated using s_1 and s_3 show much lower forward current even with a large value of s_1 and s_3 (i.e., 1×10^8 cm/s). The slope of the two plots indicates that the currents with s_1 and s_3 are dominated by bulk diffusion current under low-level injection. This result leads to the conclusion that the forward current of a GaN mesa-type p$^+$n diode is dominated by s_2, namely, carrier recombination at the side surface of the etched n-GaN.

3.7.2 Influence of Electric-Field Concentration on Non-Self-Aligned Mea-type p$^+$n Diodes

Here we analyze another multidimensional effect concerning a highly forward-biased p$^+$n junction. To exclude the influences of deep acceptors in GaN and 4H-SiC (see Section 2.4.2) and surface recombination, a non-self-aligned mesa-type Si p$^+$n diode with an over-etched depth of zero at 300K was numerically investigated (Figure 3.10) [23]. Potential contours of the diode (anode-electrode radius: 30 μm; mesa radius: 35 μm) were simulated in terms of a cylindrical coordinate system by using the commercial simulator [21]. The epitaxial layers consist of 0.5-μm-thick Si (N_A: 5×10^{17} cm^{-3}) and 10-μm-thick Si (N_D: 2×10^{16} cm^{-3}). As for the Si substrate, a thickness of 500 μm and N_D of 5×10^{18} cm^{-3} were assumed. For both electrons and holes, the same lifetime (10 μs) was used.

Simulated potential contours of the non-self-aligned mesa-type Si p$^+$n diode are shown in Figure 3.11. When V is 0.6V, the potential variation in the n-Si layer is only 22 mV (Figure 3.11[a]). Under this bias condition, the n-Si layer is considered to be quasi-neutral, and minority-carrier diffusion dominates J_{total}. As V increases, conductivity modulation gets stronger, and the potential variation in the n-Si layer increases {i.e., 27 mV at 0.8V (Figure 3.11[b]) and 38 mV at 0.9V (Figure 3.11[c])}. Accordingly,

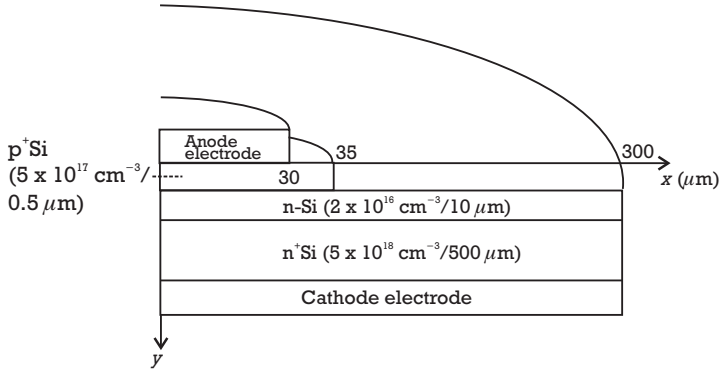

Figure 3.10 Schematic of simulated non-self-aligned mesa-type Si p^+n diode. The over-etched depth of the n-Si layer is assumed to be zero.

the n-Si layer is no longer considered to be quasi-neutral, and the drift-current component dominates J_{total}. At 0.8V, the potential contours in the n-Si layer terminate at the p-n junction.

However, at 0.9V, the potential contours in the n-Si layer extend into the p^+Si layer, and potential crowding is observed in the p^+Si layer around the edge of the anode electrode (Figure 3.11[c]). This electric-field concentration around the edge of the anode electrode leads to peak J_{total} exceeding 10^4 A/cm^2 (Figure 3.12). Such a considerable increase in J_{total} is considered to be a feature of a non-self-aligned mesa-type p^+n junction, and it plays an important role in photon recycling (described in Chapter 4).

3.8 Junction Breakdown

Under a sufficiently high electric field, one of two breakdown processes can occur. In the first one, called avalanche breakdown, free carriers gain enough energy from the field to break covalent bonds in the lattice (see Section 2.6). In the second breakdown process, called Zener breakdown, an electron makes a transition from a valence band to a conduction band without interactions of any other particles (i.e., band-to-band tunneling). Devices exhibiting Zener breakdown have lower breakdown voltage (BV) than those exhibiting avalanche breakdown. In other words, as understood from (3.30) and (3.31), small W_D (i.e., large N_D) is necessary for band-to-band tunneling to occur.

In the case of Si p-n junctions, whether avalanche or Zener breakdown occurs can be determined by temperature (T) dependence of BV; that is, with increasing T, BV increases because the mean-free path of electrons decreases (so avalanche breakdown occurs), while BV decreases because

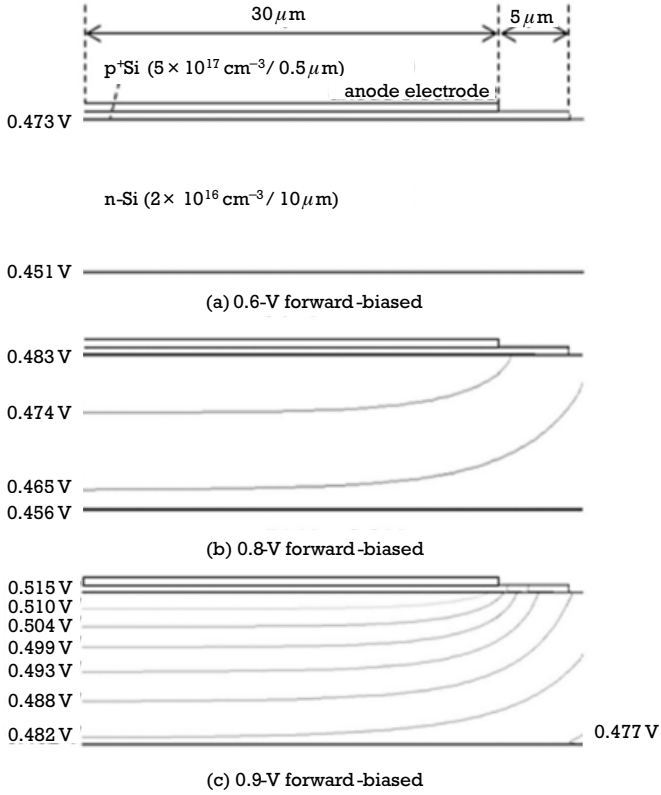

Figure 3.11 Simulated potential contours of non-self-aligned mesa-type Si p-n diode forward-biased at (a) 0.6V, (b) 0.8V, and (c) 0.9V.

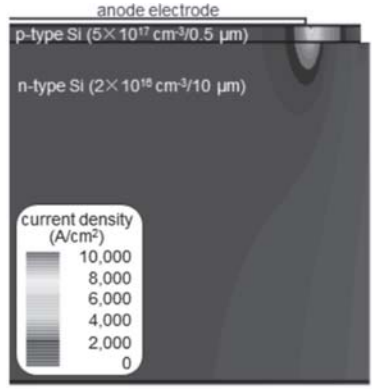

Figure 3.12 Simulated iso-current-density contours of non-self-aligned mesa-type Si p-n diode forward-biased at 0.9V.

the flux of valence-band electrons available for band-to-band tunneling increases (so Zener breakdown occurs). However, this trend is not necessarily true for p-n junctions made of GaN and 4H-SiC having a relatively large density of crystal defects. For example, in the case of 4H-SiC p-n junctions, the reported dependence of *BV* on *T* varied from junction to junction [24].

3.9 Summary

This chapter compares carrier recombination lifetimes and current/voltage characteristics of GaN and 4H-SiC p-n junctions with those of a Si p-n junction. Among the multidimensional effects the chapter introduces, electric-field concentration around the edge of a non-self-aligned mesa-type p-n junction is described—to the author's knowledge, for the first time in semiconductor textbooks. Such electric-field concentration leads to large local current density, which is considered to be the basis for photon recycling to occur in direct-bandgap semiconductors (see Chapter 4).

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CHAPTER

4

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Effects of Photon Recycling

4.1 Introduction

It is often said that GaN is not suitable for bipolar power devices because it is a direct-bandgap semiconductor (see Section 2.3) so that it could have a short carrier recombination lifetime (see Section 3.4). For example, in [1], Baliga wrote, "the interest in GaN power devices is limited to unipolar power devices." In the same textbook, however, he referred to the reported 3.7-kV GaN p-n diodes [2] and wrote, "The diodes exhibited the expected knee voltage of 3.0 volts and an on-state voltage drop of 3.3 volts at a current density of 100 A/cm^2. The low on-state voltage drop was observed despite a very low lifetime of 2 ns measured in the drift region." [3] Although the reason for the low on-state voltage drop is not described in the textbook, it is attributable to the increased carrier recombination lifetime due to photon recycling. Gaining advantage from photon recycling is indispensable for improving the performance of

GaN p-n diodes (see Section 10.3) and GaN bipolar junction transistors (see Section 10.5.4).

As described in Sections 2.3 and 3.4, photon recycling is the reabsorption of recombination radiation in direct-bandgap semiconductors such as GaN, GaAs, and $Al_xGa_{1-x}As$ ($x < 0.4$) [4, 5]. Its effect in indirect-bandgap semiconductors, such as SiC and silicon, is thus considered to be negligible. With respect to AlGaAs-GaAs heterostructures, the influence of photon recycling on radiative-recombination lifetime [6], diffusion length and internal quantum efficiency [7], and minority-carrier lifetime [8] has been investigated; and photon recycling was first utilized in semiconductor devices for reducing the threshold currents of ridge [9] and surface-emitting laser diodes [10] in 1990 and 1991, respectively. In 2011, photon recycling was also utilized for improving performance of GaAs solar cells and vertical GaN p-n diodes; in particular, a conversion efficiency η of 28.2%, beating the previous record of 26.4% [11], and low differential specific on-resistance $R_{on}A^{diff}$ (Section 1.3.2), independent of temperature [12], were achieved. Since then, photon recycling has been applied to multijunction solar cells and GaN p-n diodes with breakdown voltage BV exceeding 3 kV; for example, in 2013, both η of two-junction nonconcentrator solar cells and figure-of-merit $BV^2/R_{on}A^{diff}$ of GaN p-n diodes rapidly deviated from their respective long-term trends [13–22] (Figure 4.1). However, the detailed mechanisms of photon recycling in the case of these solar cells and p-n diodes are considered to be different. This chapter breaks photon

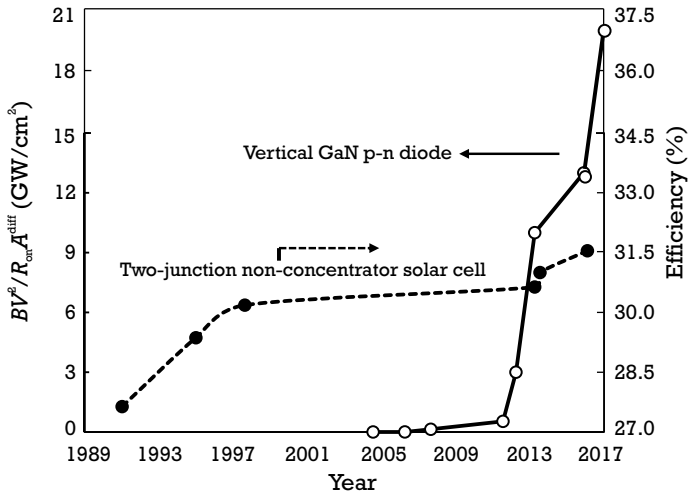

Figure 4.1 Conversion efficiency of two-junction nonconcentrator GaAs solar cells and the ratio of the square of breakdown voltage (BV) to differential on-resistance ($R_{on}A^{diff}$) of vertical GaN p-n diodes as a function of the year of publication.

recycling into separate types and models these on the basis of experimental findings.

4.2 Family Tree of Photon-Recycling Phenomena

Photon recycling can be distinguished by the way emitted photons are recycled (Figure 4.2). In the case of external photon recycling, as shown schematically in Figure 4.3(a), parts of the photons (with energy $h\nu_1$) that are emitted externally from active region 1 are recycled in narrower-bandgap active region 2; that is, the emitted photons are absorbed in active region 2 and create electron-hole pairs; the created electrons and holes rapidly emit phonons (namely, thermalize to the band edge); and recombination of the electrons at the bottom of the conduction band (E_{C2}) and the holes at the top of the valence band (E_{V2}) results in the emission of photons with energy $h\nu_2$ (which is lower than $h\nu_1$) (Figure 4.3[b]).

Using blue-spectral InGaN in active region 1 and yellow-spectral AlGaInP in active region 2, an externally photon-recycled white light-emitting diode (LED) was first demonstrated in 1999 [23]. The latest achievement concerning external photon recycling include a safe ultraviolet (UV) LED. Since UV light is invisible to the naked eye and may cause irreparable damage to the human skin and eyes, green-light emission was incorporated

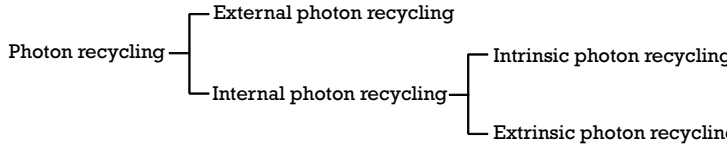

Figure 4.2 Family tree of photon-recycling phenomena.

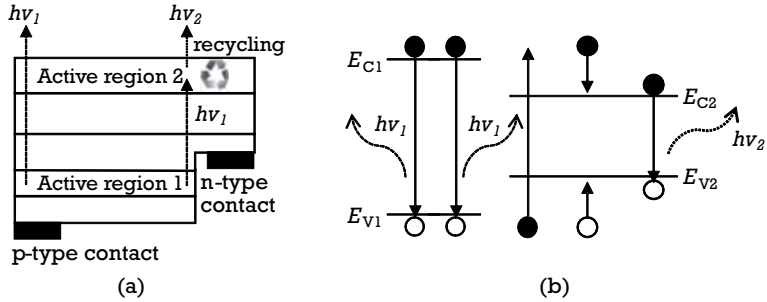

Figure 4.3 (a) Schematic cross-section of a "semiconductor photon-recycling light-emitting diode" [23] and (b) energy-band diagrams illustrating processes involved in external photon recycling.

in that UV LED as an indicator and warning sign during operation. Using ultraviolet-spectral $In_{0.01}Ga_{0.99}N$ in active region 1 and green-spectral $In_{0.28}Ga_{0.72}N$ in active region 2, a UV LED with an externally photon-recycled green indicator was demonstrated [24].

Internal photon recycling, in which the emitted photons are recycled within the host crystal, can be categorized as intrinsic photon recycling (IPR) by band-to-band transitions and extrinsic photon recycling (EPR) by transitions involving forbidden-gap energy levels [25]. As shown as an example of a forward-biased p^+-n direct-bandgap semiconductor junction in Figure 4.4, intrinsic photon recycling increases minority-carrier lifetime τ_p; that is, the ratio of the resultant effective minority-carrier lifetime τ_{eff} to τ_p is defined as photon-recycling factor Φ [6] (see Section 3.4.4). Note that Φ should be different for specific device structures; for example, $\Phi = 4–6$ in the case of an AlGaAs/8-μm-thick GaAs/AlGaAs double heterostructure [8]. On the other hand, extrinsic photon recycling involving deep acceptors or deep donors increases the ionization ratio of those dopants. However, the mechanism for extrinsic photon recycling has yet to be established. Section 4.7 presents possible models based on indirect experimental evidence.

4.3 Intrinsic Photon Recycling

The effect of intrinsic photon recycling on vertical GaN p-n diodes was analytically estimated by Velmre and Udal [26]. However, before their work is discussed, the effect of intrinsic photon recycling in GaAs solar cells is examined. By equating the ideal diffusion current (with an ideality factor n of unity—see Section 3.6.1.1) with photocurrent I_{ph}, it is possible to express open-circuit voltage V_{OC} as [27]

$$V_{OC} = (k\,T/q)\,\ln(I_{ph}/I_S) \tag{4.1}$$

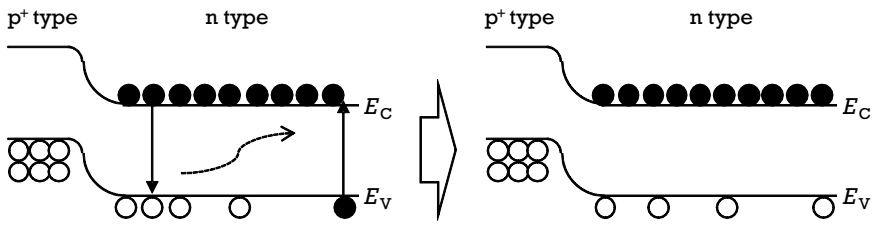

Figure 4.4 Schematic band diagrams of a forward-biased p^+-n junction where intrinsic photon recycling is taking place.

where k is Boltzmann's constant, T is absolute temperature, q is electronic charge, and I_S is saturation current. For p^+-n type and n^+-p type diodes, I_S is, respectively, given as [27]

$$I_S = (A\ q\ N_C\ N_V/N_D)\ (D_p/\tau_p^{eff})^{0.5} \exp(-E_g/k\ T) \tag{4.2a}$$

and

$$I_S = (A\ q\ N_C\ N_V/N_A)\ (D_n/\tau_n^{eff})^{0.5} \exp(-E_g/k\ T) \tag{4.2b}$$

where A is active area, N_C is effective density of states in conduction band, N_V is effective density of states in valence band, N_D is donor density, N_A is acceptor density, D_p is hole diffusivity, D_n is electron diffusivity, τ_p^{eff} is effective hole lifetime, τ_n^{eff} is effective electron lifetime, and E_g is energy bandgap. As the influence of intrinsic photon recycling increases, τ_p^{eff} or τ_n^{eff} increases, thereby decreasing I_S and increasing V_{OC}.

For example, in 2011, a GaAs single-junction solar cell with record η, consisting of front-metal contacts, an antireflection coating, a back-metal contact, and a flexible handle (Figure 4.5), attained I_S/A of 6.0×10^{-21} A/m^2 [28]. According to (4.2a) under the simple assumption of $\Phi = 10$, I_S/A should be $6.0 \times 10^{-21} \times 10^{0.5} = 1.9 \times 10^{-20}$ (A/m^2) when the effect of intrinsic photon recycling is negligible (Figure 4.6[a]). Current/voltage characteristics of the GaAs solar cell under illumination are shown in Figure 4.6(b), where the solid and dashed curves, respectively, denote the characteristics with and without intrinsic photon recycling. Note that intrinsic photon recycling affects V_{OC}, but not short-circuit current I_{SC}. Therefore, the maximum output power with intrinsic photon recycling becomes larger than maximum output power without intrinsic photon recycling (i.e., area $V_m^{w.o.PR}\ I_m$ of the rectangle with hatched dashed lines in Figure 4.6[b] by area $(V_m - V_m^{w.o.PR})$ I_m of the rectangle with hatched solid lines in Figure 4.6[b]).

As for the increase in η of a two-junction solar cell reported in 2013 (Figure 4.1), intrinsic photon recycling also played an important role [29]. As shown in Figure 4.7, radiative recombination in the bottom (GaAs) cell

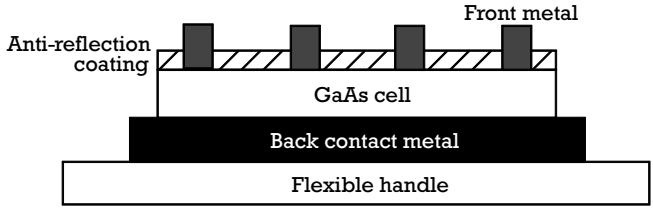

Figure 4.5 Schematic cross-section of reported GaAs single-junction solar cell [28].

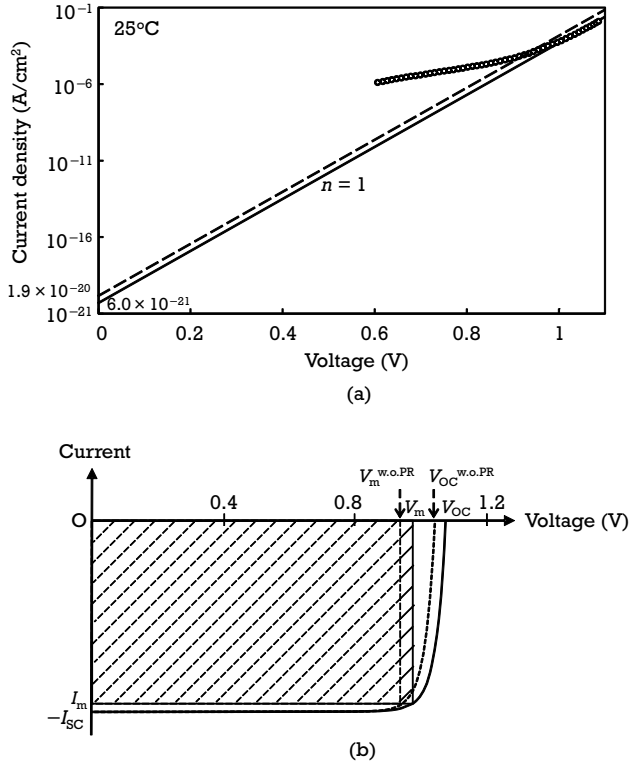

Figure 4.6 (a) Dark current-density/voltage characteristics and (b) illuminated current/voltage characteristics of a GaAs single-junction solar cell shown in Figure 4.5. In (a), open circles denote series-resistance-corrected data [28]; solid and dashed lines, respectively, denote ideal diffusion-current density (whose ideality factor n is unity) with and without intrinsic photon recycling. In (b), solid and dashed curves, respectively, denote characteristics with and without intrinsic photon recycling. I_m and V_m correspond to current and voltage for maximum power output (I_{SC}: short-circuit current [i.e., photocurrent I_{ph}]; V_{OC}: open-circuit voltage with effect of photon recycling; $V_{OC}^{w.o.PR}$: open-circuit voltage without effect of photon recycling).

leads to the emission of photons at approximately the bandgap energy of GaAs (shown by solid arrows). Efficient photon recycling is possible because these photons are not absorbed in the top cell (made of wider-bandgap InGaP). It has to be noted, however, that the photons emitted through radiative recombination in the InGaP cell (shown by dashed arrows) are strongly absorbed in the GaAs cell, and that absorption reduces the potential for intrinsic photon recycling within the InGaP cell.

The effect of intrinsic photon recycling on vertical GaN p-n diodes was similarly analyzed by Velmre and Udal [26]. However, their analyses

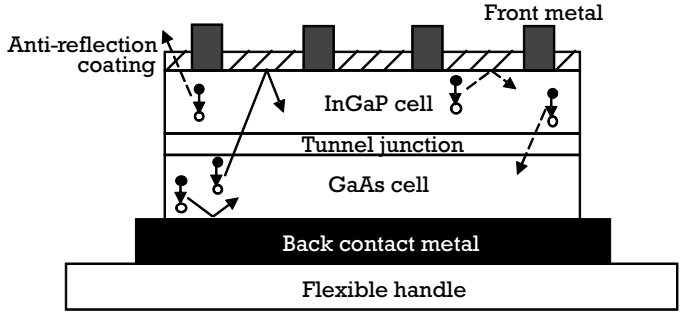

Figure 4.7 Schematic cross-section of reported InGaP/GaAs two-junction solar cell [29].

were carried out before forward-current (I_F)/voltage (V_F) characteristics of vertical GaN p-n diodes were reported. Section 4.4 shows that the measured I_F/V_F characteristics of vertical GaN p-n diodes cannot be reproduced by simulation including the effect of intrinsic photon recycling only.

4.4 Influence of IPR on Forward-Biased GaN p-n Diodes

The I_F/V_F characteristics of a non-self-aligned mesa-type GaN p-n diode (anode-electrode radius: 30 μm; mesa radius: 35 μm) (Figure 4.8) were simulated (in terms of the cylindrical coordinate system) by using the commercial device simulator [30]. The epitaxial layers consisted of 0.5-μm-thick GaN (acceptor concentration N_A: 5×10^{17} cm^{-3}; acceptor level E_A: 0.235 eV [31]) and 10-μm-thick GaN (donor concentration N_D: 2×10^{16} cm^{-3}). As for the GaN substrate, a thickness of 500 μm and N_D of 5×10^{18} cm^{-3} were assumed. For lifetime τ of both electrons and holes, the same value was used. Contact resistivities of the anode and cathode electrodes were neglected.

As shown in Figure 4.9, I_F of GaN p-n diodes increases with increasing τ; however, I_F saturates when τ exceeds 0.5 ms, and saturated I_F is lower than measured I_F (solid circles in Figure 4.9 [18]) when V_F exceeds 3.6V. This result shows that the extended τ due to intrinsic photon recycling does not play a dominant role in determining the I_F of vertical GaN p-n diodes. In contrast, even with τ of 50 ns, simulated I_F monotonically increases with decreasing E_A; in other words, the simulation can reproduce measured I_F with E_A between 0.135 and 0.185 eV (Figure 4.10). This result indicates that forward-current conduction increases the ionization ratio of deep acceptors with an E_A of 0.235 eV. Since forward-current conduction generates not only recombination radiation but also heat, Section 4.5 considers the self-heating effect on the measured I_F.

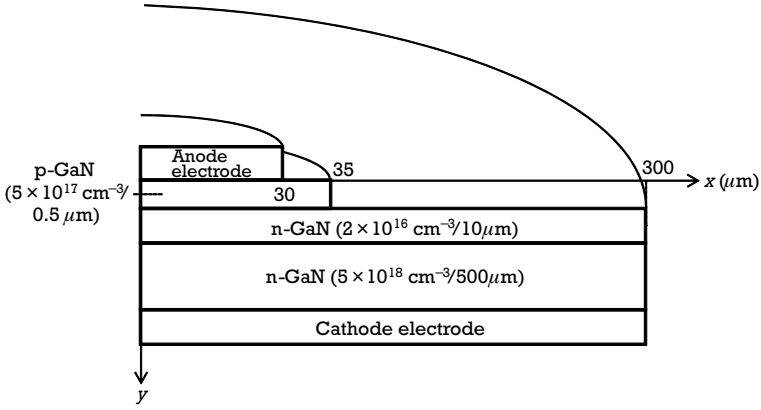

Figure 4.8 Schematic of a simulated non-self-aligned mesa-type GaN p-n diode.

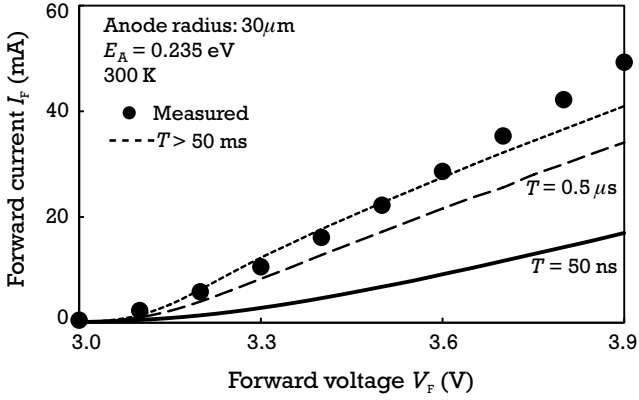

Figure 4.9 Measured forward-current/voltage characteristics of the GaN p-n diode reported in [18] (circles), together with characteristics simulated with a minority-carrier lifetime τ of 50 ns (solid line), 0.5 μs (dashed line), and 50 ms or longer (dotted line).

4.5 Influence of Self-Heating on Forward-Biased GaN p-n Diodes

The self-heating effect on GaN-based high-power transistors was investigated by Turin and Balandin using the method of images [32]. They calculated the heat-spreading radius (b) from a point heat source on the surface of a substrate (thermal conductivity: κ_1; thickness: t) with its rear surface contacting a heat sink (thermal conductivity: κ_2) (Figure 4.11[a]). When $\kappa_2/\kappa_1 > 10$, the amount of normalized heat flow $2b/t$ does not depend on κ_2/κ_1 but on the net heat-flow fraction (Σ in Figure 4.11) only; that is, $2b/t = 2.0$, 2.3, and 2.8, when $\Sigma = 50$, 60, and 70%, respectively [32]. When the heat

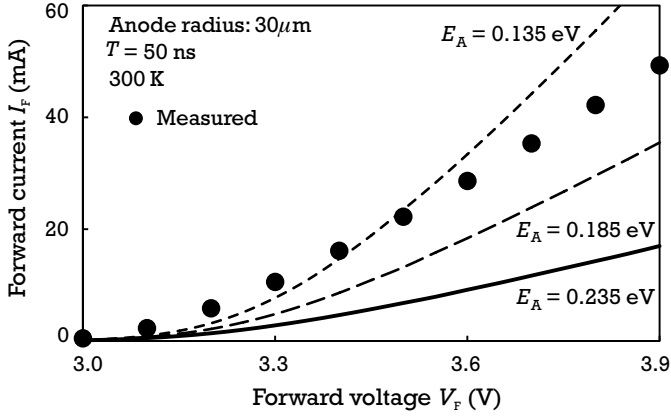

Figure 4.10 Measured forward-current/voltage characteristics of the GaN p-n diode reported in [18] (circles), together with characteristics simulated with acceptor level E_A of 0.235 eV (solid line), 0.185 eV (dashed line), and 0.135 eV (dotted line).

source has a finite area (radius: a), as shown in Figure 4.11(b), thermal resistance (R_{th}) across a circular cross-section (radius: b) along the vertical axis (z-axis) can be obtained, as long as heat spreads uniformly in the circular truncated cone, as follows [33]:

$$R_{th} = \int_{at/(b-a)}^{bt/(b-a)} (1-\kappa_1) t^2 \left[\pi(b-a)^2\right] z^{-2} dz = \left[2/(\pi\kappa_1 a)\right]/(2b/t) \tag{4.3}$$

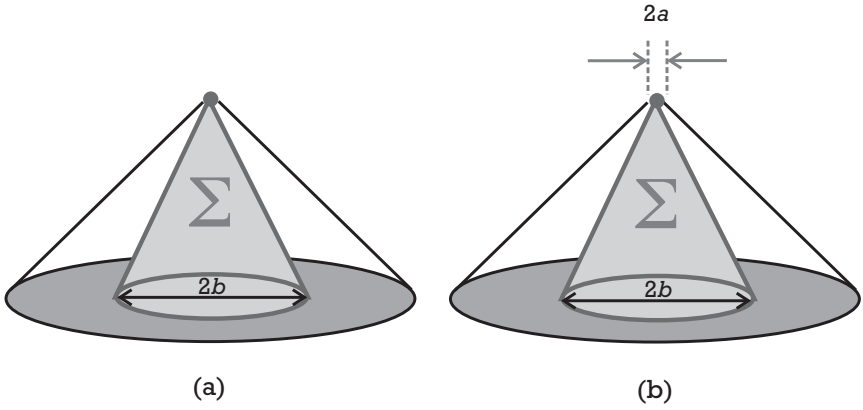

Figure 4.11 Schematic of net heat-flow fraction Σ from (a) point and (b) circular (radius: a) heat sources on the surface of a semiconductor substrate.

The increase in junction temperature T_j (ΔT_j) of GaN p–n diodes can therefore be estimated if a is small. When a is 30 μm, putting measured k_l of 2.0 $Wcm^{-1}K^{-1}$ [34] into (4.3) gives

$$R_{th}\ (W/K) = 106 / (2b/t) \tag{4.4}$$

As shown in Figures 4.9 and 4.10, at 300K, power consumed by the diode (P) was 0.192W when the diode was forward-biased at 3.9V. When the ratio of photons externally radiated from the mesa edge is η_e, the net power that increases T_j is $(1 - \eta_e)P$; ΔT_j is thus expressed as

$$\Delta T_j = 20\ \Sigma\ (1 - \eta_e)/\ (2b/t) \tag{4.5}$$

Since determining η_e requires integrating sphere measurements, ΔT_j was calculated as a function of η_e instead. As shown in Figure 4.12, maximum ΔT_j is 5.2 K at $\eta_e = 0$ and almost independent of Σ (in the range from 50 to 70%). This ΔT_j value is concluded to be too small to increase acceptor ionization at 300K. Therefore, the possible increase of ionization ratio of deep acceptors described in Section 4.4 is attributable to radiative recombination, namely, extrinsic photon recycling.

4.6 Influence of EPR on Forward-Biased GaN p-n Diodes

As shown in Section 3.7, peripheral current dominates I_F of highly forward-biased non-self-aligned p-n diodes. Therefore, the E_A values used to

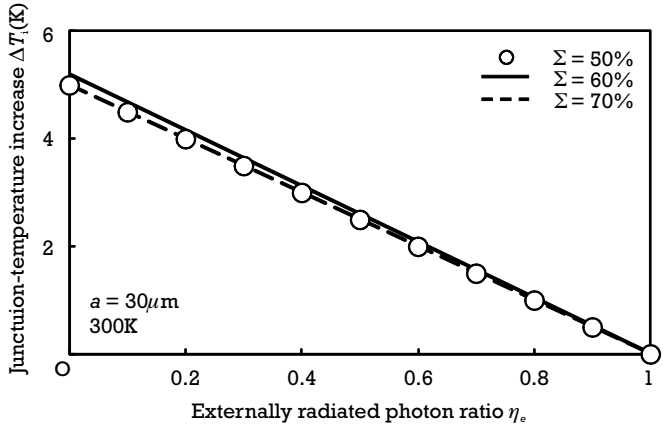

Figure 4.12 Dependence of estimated increase in junction temperature of the GaN p-n diode shown in Figure 4.8 on an externally radiated photon ratio. Net heat-flow fraction Σ is varied from 50 to 70%.

reproduce measured I_F of the GaN p-n diode in Figure 4.10 can only be used as a guide for an effective acceptor level E_A^{eff}. To quantitatively evaluate E_A^{eff} due to extrinsic photon recycling, rectangular transmission-line-model (TLM) patterns [35] formed with GaN p^+–n junction epitaxial layers were employed by Mochizuki et al. [36]. Instead of E_A = 0.175 eV [37] used in [36], more recently reported E_A of 0.235 eV [31] is used in the following.

The mesa structure of the TLM patterns (Figures 4.13 and 4.14), with epitaxial layer structures consisting of p^{++}-GaN (Mg: 2×10^{20} cm^{-3}/20 nm)/ p^+-GaN (Mg: 5×10^{17} cm^{-3}/0.5 μm)/n^--GaN (Si: 2×10^{16} cm^{-3}/10 μm)/ n^+-GaN (Si: 2×10^{18} cm^{-3}/ 2 μm), was fabricated by inductively coupled-plasma (ICP) dry etching (see Section 7.2). Titanium/aluminum and palladium/aluminum ohmic electrodes, respectively, were then formed by electron-beam deposition on the bottom surface of an n^+-GaN substrate and on the top surface of a p^{++}-GaN layer (see Section 7.6.1). Finally, the exposed portion of the p^{++}-GaN layer was etched by ICP dry etching using the palladium/aluminum electrodes as a mask. Current/voltage characteristics of the fabricated TLM patterns were first measured conventionally (namely, with no bias applied to the p–n junction; see Figure 4.13[b]). Under the

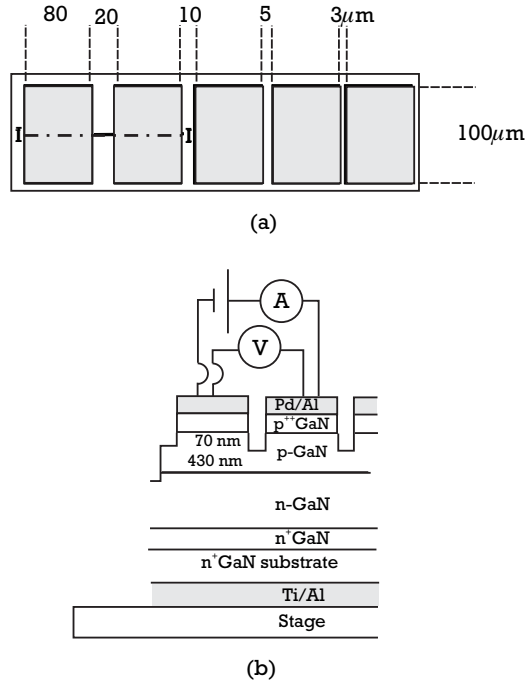

Figure 4.13 Schematic (a) plan view of TLM patterns and (b) I-I cross-section of conventional TLM measurement setup.

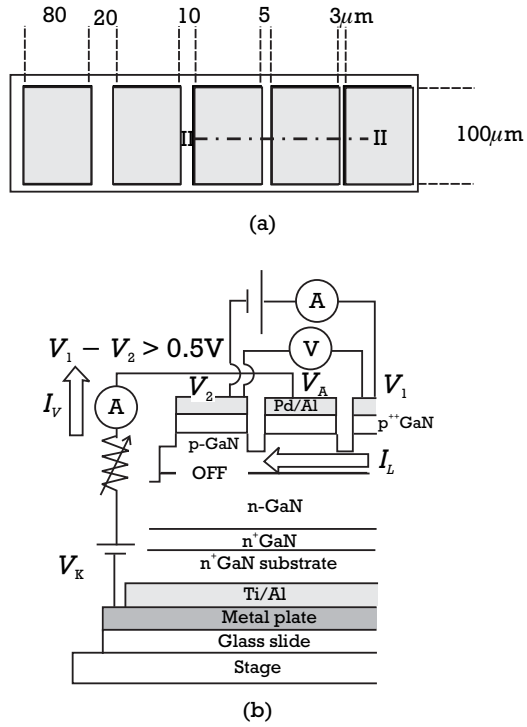

Figure 4.14 Schematic (a) plan view of transmission-line-model (TLM) patterns and (b) II-II cross-section of forward-biased TLM measurement setup.

assumption that the resistance of the pattern with the largest gap (i.e., 20 μm) is dominated by the sheet resistance of the p$^+$-GaN layer, hole mobility μ_p was determined to be 15 cm^2/Vs from the current/voltage characteristics obtained by the commercial device simulator [30] (Figure 4.15).

One of the palladium/aluminum electrodes (anode) was then forward-biased to the bottom electrode (cathode), and the current/voltage characteristics between the electrodes on both sides (Figure 4.14) were measured. As shown in Figure 4.16 as an example of potentials V_1 and V_2 simulated with anode current of 90 mA in 3-μm-gap/5-μm-gap patterns shown in Figure 4.14, V_1 is almost constant, and V_2 linearly decreases with increasing $|V_1 - V_2|$ when $V_1 - V_2 > 0.5$V. Under this condition, lateral-current ($|I_L|$)/lateral-voltage ($|V_1 - V_2|$) characteristics of the 5-μm-gap region in the p$^+$-GaN layer are obtained. In Figure 4.16, when $V_1 - V_2 < -0.5$V, on the other hand, V_2 is almost constant, and V_1 linearly decreases with increasing $|V_1 - V_2|$. Under this condition, $|I_L|/|V_1 - V_2|$ characteristics of the 3-μm-gap region in the p$^+$-GaN layer are obtained.

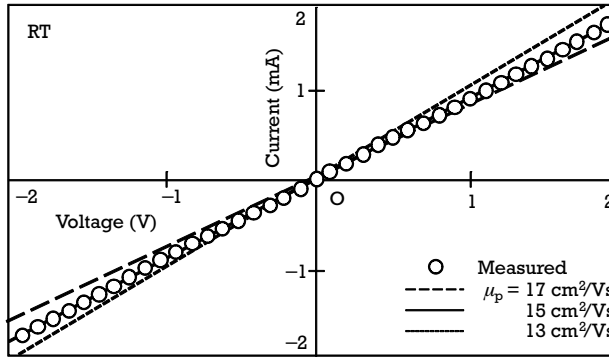

Figure 4.15 Measured (open circles) and simulated (by using hole mobility μ_p as a parameter) current/voltage characteristics of a 20-μm-gap transmission-line-model pattern.

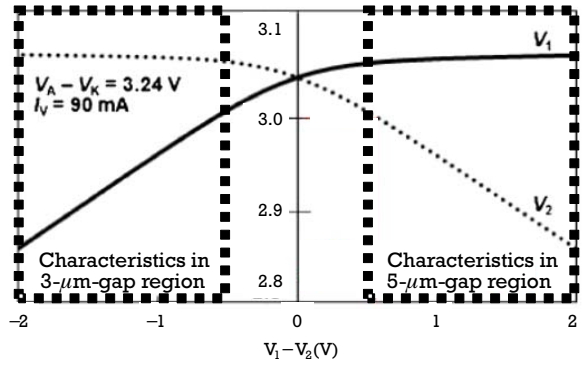

Figure 4.16 Simulated potentials of V_1 and V_2 (in Figure 4.14) of 3-μm-gap/5-μm-gap patterns with anode current of 90 mA (i.e., anode-to-cathode voltage [$V_A - V_K$ in Figure 4.14] of 3.24V), as a function of V_1 - V_2.

When $|V_1 - V_2| < 0.5$V, both V_1 and V_2 are larger than the built-in potential of the p–n junction, V_{bi} (about 3V), so the hole current flows not only in the p$^+$-layer but also in the n$^-$-GaN layer. Therefore, the experimental results for this condition ($|V_1 - V_2| < 0.5$V) were not used because of difficulty in the analysis.

Measured and simulated $|I_L|/|V_1 - V_2|$ characteristics of the TLM patterns when the vertical anode current I_V was 90 mA are compared in Figure 4.17. When the gap of the TLM patterns is 20 μm (Figure 4.17[a]), measured I_L agrees well with I_L simulated with an E_A of 0.235 eV. However, as the gap decreases from 10 μm, measured I_L deviates more from I_L simulated with E_A of 0.235 eV. (Figure 4.17[b–d]). Since this tendency was also the case for

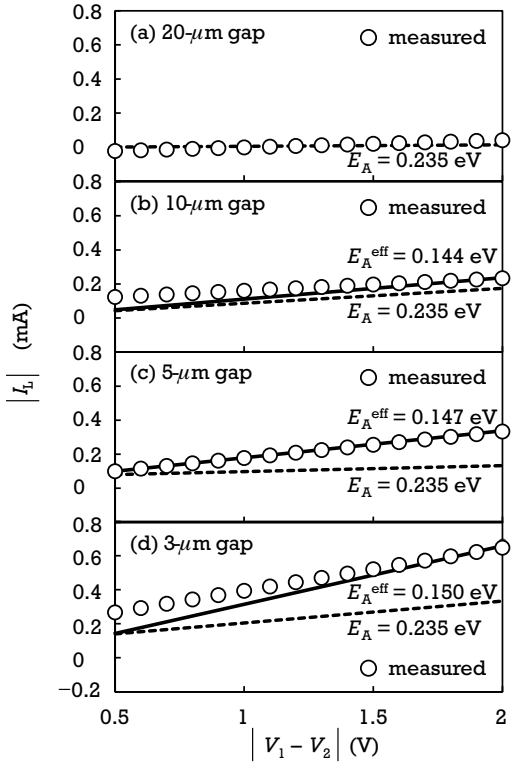

Figure 4.17 Measured (symbols) and simulated lateral-current ($|I_L|$)/lateral-voltage ($|V_1–V_2|$) characteristics of transmission-line-model patterns with vertical current of 90 mA.

I_V = 10–70 mA, it is concluded that the effect of extrinsic photon recycling rapidly decreases from the edge of the p-type electrode, over a 10-μm range, independently of I_V.

4.7 Possible Models for EPR

In a conductivity-modulated GaN p^+-n junction (see Section 3.7), photons are considered to be created mainly through the conduction-band/valence-band transition in n-GaN. In [33], the energy of photons was assumed to be used for electron emission from ionized magnesium acceptors to the conduction band (Figure 4.18[a-1]). The resultant neutralized acceptors are then ionized through electron capture from the valence band. The electrons emitted from the ionized magnesium acceptors to the conduction band in p^+-GaN are considered to emit phonons and move to the conduction-band minimum (Figure 4.18[a-2]). If the holes are injected into n-GaN (Figure

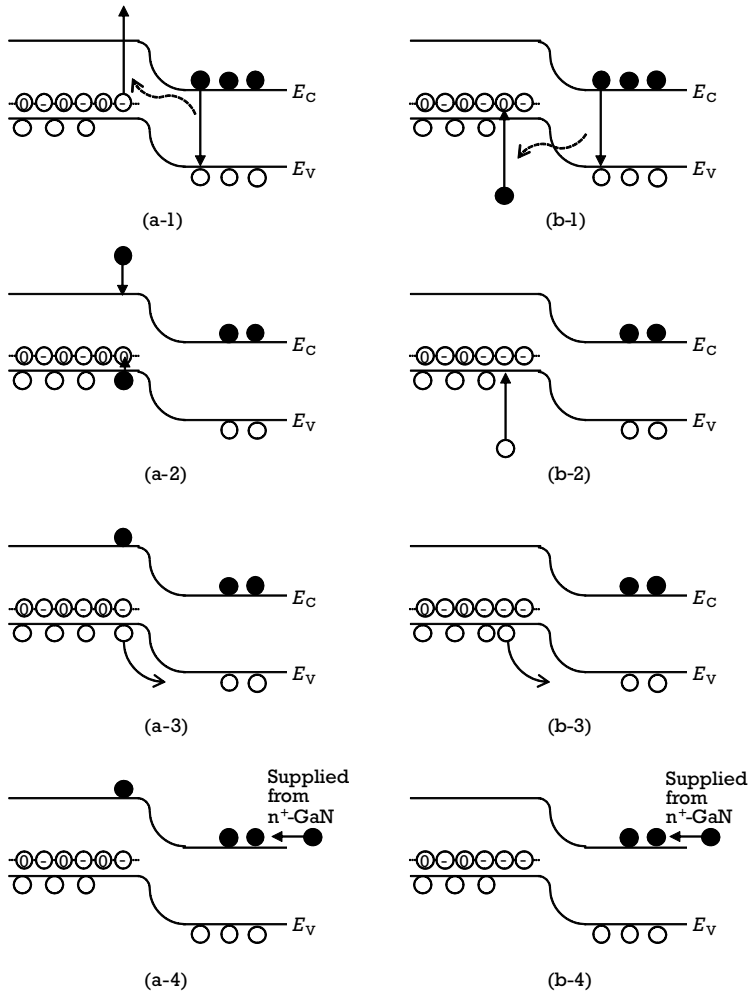

Figure 4.18 Energy-band diagrams illustrating two possible models (i.e., from [a-1] to [a-4] and from [b-1] to [b-4] for extrinsic photon recycling in GaN p-n diodes.

4.18[a-3]), the same number of electrons are injected into n-GaN from n^+-GaN to maintain charge neutrality in n-GaN (Figure 4.18[a-4]). However, if the electrons recombine with the holes in p^+-GaN, the ratio of ionized magnesium acceptors does not increase.

If the energy of photons was used by neutral magnesium acceptors to capture electrons from the valence band (Figure 4.18[b-1]), the acceptors are ionized and the high-energy holes in the conduction band in p^+-GaN are considered to emit phonons and move to the valence-band maximum (Figure 4.18[b-2]). In this case, the ratio of ionized magnesium acceptors increases. And if the holes are injected into n-GaN (Figure 4.18[b-3]), to

maintain charge neutrality in n-GaN, the same number of electrons are injected into n-GaN from n^+-GaN (Figure 4.18[b-4]).

Note that in both cases shown in Figure 4.18(a-1–a-4, b-1–b-4), conservation of momentum is not violated; since acceptors and donors are highly localized, they have a wide range in momentum space (according to the uncertainty principle). To reveal the mechanism of extrinsic photon recycling, however, further experimental investigation is needed.

4.8 Summary

This chapter classifies photon recycling as external photon recycling or internal photon recycling. White and UV LEDs are introduced as examples of the application of external photon recycling. Internal photon recycling, which has recently been utilized to improve the η of multijunction solar cells and $BV^2/R_{on}A^{diff}$ of vertical GaN p-n diodes, was further classified as intrinsic photon recycling by band-to-band transitions and extrinsic photon recycling by transitions involving forbidden-gap energy levels. While intrinsic photon recycling is responsible for improving η, intrinsic photon recycling alone cannot explain the improved $BV^2/R_{on}A^{diff}$. Extrinsic photon recycling by transitions involving deep acceptors is thus considered to play an important role in increasing the ionization ratio of deep acceptors in p^+-GaN. To reveal the mechanism of extrinsic photon recycling, however, further experimental investigation is needed.

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CHAPTER

5

Contents

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5.9 Summary

Bulk Crystal Growth

5.1 Introduction

Growing bulk crystals is indispensable for producing single-crystal wafers. It is well-known that silicon wafers are produced from a polycrystalline silicon melt. Even in the case of GaAs, which has a considerable vapor pressure due to arsenic, melt growth with a liquid encapsulant (i.e., boron oxide, B_2O_3) has been widely used for producing single-crystal wafers [1]. However, no such encapsulant for either GaN or SiC has been found.

As shown in the phase diagrams of the GaN and SiC binary systems in Figure 5.1, a stoichiometric liquid phase does not exist in GaN or SiC under atmospheric pressure [2, 3]. For liquid-phase bulk growth from a stoichiometric melt, temperature and pressure exceeding, respectively, 2,700K and 92,000 atm for GaN (Figure 5.2 [2]) and 3,573K and 98,000 atm for SiC [3] are theoretically needed. Therefore, the most common techniques for growing bulk GaN and SiC at present is vapor-phase growth—namely,

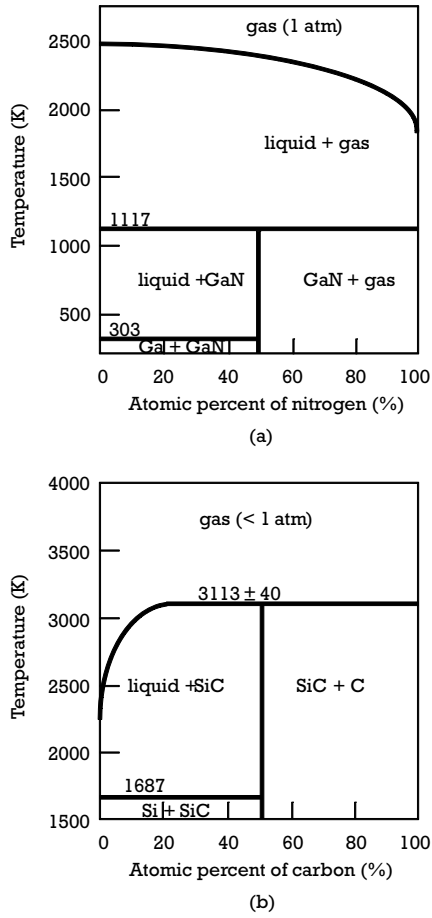

Figure 5.1 Phase diagrams of (a) GaN and (b) SiC binary systems under atmospheric pressure [2, 3].

hydride vapor-phase epitaxy (HVPE) for growing GaN and sublimation for growing SiC. This chapter also introduces other techniques for bulk-crystal growth, as they are now being intensively investigated as ways to improve crystal quality and productivity.

5.2 HVPE Growth of GaN

Since GaN seed crystal is not readily available (see Section 2.1), thick GaN films are grown by HVPE on foreign substrates, such as GaAs and sapphire. The biggest advantage of HVPE growth is its high growth rate (typically, several hundred micrometers per hour).

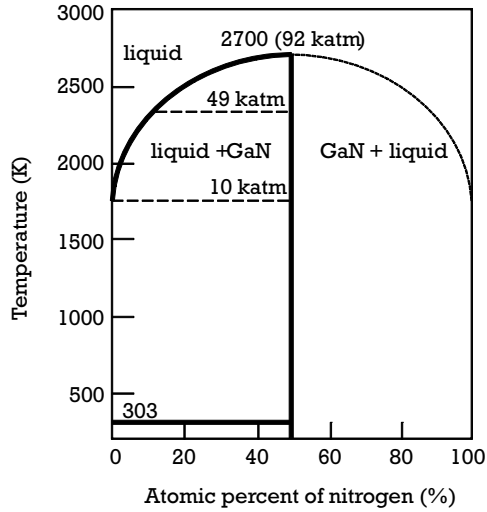

Figure 5.2 Calculated condensed phase diagram of the GaN system [2].

5.2.1 Mechanism of HVPE Growth of GaN

An HVPE reactor generally consists of source and epitaxy zones (Figure 5.3). In the source zone, gallium is kept at a certain temperature (about 1,100K) and reacts with HCl gas as follows:

$$2Ga(l)+2HCl(g) \leftrightarrow 2GaCl(g)+H_2(g) \quad (5.1a)$$

$$Ga(l)+HCl(g) \leftrightarrow GaCl_2(g)+H_2(g), \quad (5.1b)$$

$$2Ga(l)+6HCl(g) \leftrightarrow 2GaCl_3(g)+3H_2(g) \quad (5.1c)$$

$$2GaCl_3(g) \leftrightarrow (GaCl_3)_2(g) \quad (5.1d)$$

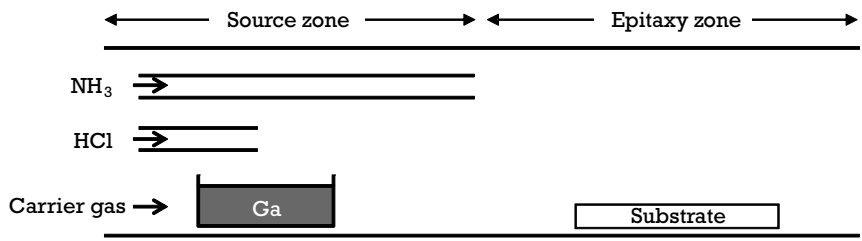

Figure 5.3 Schematic illustration of hydride vapor-phase epitaxial growth reactor consisting of source and epitaxy zones.

where "l" and "g" in parentheses denote, respectively, liquid and gas. The gaseous species formed in the source zone according to the above reactions and NH_3 are separately transported to the epitaxy zone by a carrier gas such as hydrogen, nitrogen, helium, and argon.

In the epitaxy zone, the source species are mixed according to the following reactions:

$$GaCl(g)+NH_3(g) \leftrightarrow GaN(s)+HCl(g)+H_2(g) \tag{5.2a}$$

$$2GaCl(g)+2HCl(g) \leftrightarrow 2GaCl_2(g)+H_2(g) \tag{5.2b}$$

$$GaCl(g)+2HCl(g) \leftrightarrow GaCl_3(g)+H_2(g) \tag{5.2c}$$

$$2GaCl_3(g) \leftrightarrow (GaCl_3)_2(g) \tag{5.2d}$$

where "s" in parentheses denotes solid. According to a reported thermodynamic calculation [4], the partial pressures of $GaCl_2$ and $(GaCl_3)_2$ are very small. Moreover, the partial pressure of $GaCl_3$ is much lower than that of GaCl [5], so (5.2a) is considered the most dominant reaction.

Supersaturation in the case of HVPE growth of GaN is expressed as

$$\sigma = (P^0{}_{GaCl}-P^e{}_{GaCl})/P^e{}_{GaCl} = (P^0{}_{GaCl}/P^e{}_{GaCl})-1 \tag{5.3}$$

where $P^0{}_{GaCl}$ and $P^e{}_{GaCl}$ are, respectively, input and equilibrium partial pressures of GaCl.

5.2.2 Doping During HVPE Growth of GaN

Dichlorosilane (SiH_2Cl_2) is commonly used for HVPE growth of silicon-doped GaN due to its high thermal stability [6]. Note that silane (SiH_4) is unsuitable for silicon doping in HVPE because it decomposes into silicon and hydrogen before it is transported to the epitaxy zone. With respect to p-type doping, on the other hand, metallic magnesium has been used to fabricate freestanding GaN by HVPE [7].

5.2.3 Epitaxial Lateral Overgrowth of GaN

Epitaxial lateral overgrowth (ELO) is generally known to be effective for bending dislocations (extending from substrates) and thereby reducing dislocation density [8]. In the case of GaN, conventional ELO was improved by two processes: dislocation elimination using epitaxial growth with inverse-pyramidal pits (DEEP) [9, 10] and void-assisted separation (VAS) with a thin TiN film [11, 12].

As for DEEP [10], a SiO_2 layer having round openings was formed directly on a GaAs surface. First, a GaN buffer layer was grown on the GaAs surface at a low temperature. The substrate temperature was then raised to the growth temperature of GaN in an NH_3 ambient, and a thick GaN layer was grown. After the GaN layer was grown to a thickness of over 500 μm, the GaAs starting substrate was mechanically removed. When a GaN crystal grows with numerous large pits, dislocations are concentrated at the center of each pit. Dislocation density therefore decreases with increasing distance from the center of the pits. Up to 150-mm freestanding GaN substrates have been grown by using 150-mm GaAs wafers [13].

In contrast, dislocation density (about 3×10^6 cm^{-2}) in GaN substrates fabricated by VAS using a sapphire substrate is relatively uniform [12]. A TiN nano-mask formed during VAS is used to easily separate GaN from sapphire [11]. However, enlarging wafer diameter is difficult due to orientation deviation. Recently, 175-mm freestanding GaN substrates were fabricated by a tiling technique that merges small multiple wafers with a thick GaN layer grown by HVPE [14].

5.3 High-Pressure Nitrogen Solution Growth of GaN

In high-pressure nitrogen solution (HPNS) growth [15], the solubility of nitrogen in a gallium melt becomes relatively high, because nitrogen molecules dissociate on the gallium surface and dissolve in the gallium melt. The dissolved nitrogen atoms are then transported from hot regions to cool regions in the gallium solution, where GaN crystallizes. The growth rate is low due to the very low solubility of nitrogen (< 0.5%), and the size of the grown GaN crystals has been limited to several millimeters. However, it was reported that HPNS growth produces very low dislocation-density ($< 2 \times 10^2$ cm^{-2}) [15].

5.4 Sodium-Flux Growth of GaN

The solubility of nitrogen in a gallium melt is increased by adding sodium to the melt. This so-called sodium-flux method can thus decrease the growth-temperature range (800–1,200K) and pressure (< 50 atm) [16]. Nitrogen molecules are first ionized by sodium at the gas/liquid interface, and the ionized nitrogen is dissolved in the Ga-Na melt. The nitrogen atoms then combine with gallium atoms, thereby nucleating GaN crystal [16]. Most of the nitrogen atoms contribute to the growth of GaN-seed crystal at the bottom of a crucible. However, when the nitrogen concentration exceeds a critical value, liquid-phase epitaxy (LPE) occurs [17–23]. Four-inch GaN

bulk crystal [22] with low dislocation density (< 10^3 cm^{-2}) has reportedly been grown by this method [23].

5.5 Ammonothermal Growth of GaN

Ammonothermal growth of GaN involves creating a temperature gradient between a source material zone and GaN seeds. An autoclave, which is a pressure chamber used at elevated temperature, is filled with ammonia and heated to 800–900K, generating pressure in the range of 2,000–4,000 atm, which makes the ammonia a supercritical fluid (Figure 5.4). Supercritical ammonia enables transport of GaN from the source zone to the seeds, which can thereby grow [24]. To increase the solubility of GaN in supercritical ammonia, basic mineralizers (e.g., $NaNH_2$, $LiNH_2$, and KNH_2) or acidic mineralizers (e.g., NH_4Cl, NH_4Br, and NH_4I) are commonly used [25].

In 1995, a fine crystalline GaN was obtained from gallium, ammonia, and $LiNH_2$ (or KNH_2) by Dwilinski et al. [26] Moreover, GaN crystal grown with such basic mineralizers was reported to have dislocation density below 10^4 cm^{-2} [27]. With respect to acidic mineralizers, on the other hand, the first experimentally grown GaN crystal was reported in 2008, and its dislocation density was relatively high (10^6 cm^{-2}) due to the use of HVPE seeds [28].

Although the rate of ammonothermal growth of GaN improved to 344 μm/day for *c*-plane growth and 46 μm/day for *m*-plane growth [29], reducing the impurity level is still challenging; for example, concentrations of transition metal and oxygen in the GaN crystal were reported, respectively, to be less than 10^{17} cm^{-3} and in the order of 10^{19} cm^{-3} [5].

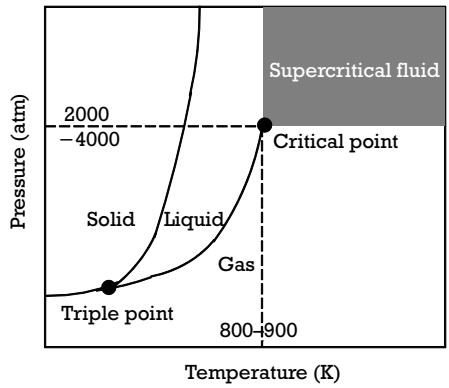

Figure 5.4 Schematic pressure versus temperature relation of ammonia.

5.6 Sublimation Growth of SiC

The first sublimation growth of SiC, in which many platelets nucleated randomly in a crucible, was carried out by Lely in 1955 [30]. After that, seeded sublimation growth of SiC, in which the seed crystal was placed at a 100-K cooler point in a crucible, was achieved by Tairov and Tsvetkov in 1978 [31]. In the case of this so-called modified Lely method, the SiC seed crystal is placed near the lid of the crucible, while SiC powder is placed at the bottom of the crucible (Figure 5.5). Radio-frequency induction or resistive heating heats the crucible, under the flow of argon or helium to about 2,600K.

Progressive increases in the diameter of sublimation-grown 4H-SiC bulk crystal has resulted in the commercial availability of 150-mm diameter wafers, as well as the recent announcement of 200-mm diameter wafers [32].

5.6.1 Mechanism of Sublimation Growth of SiC

The main reactions during sublimation growth of SiC are given as follows [33]:

$$Si_2C(g)+SiC_2(g) \leftrightarrow 3SiC(s) \tag{5.4a}$$

$$SiC_2(g)+3Si(g) \leftrightarrow 2Si_2C(g) \tag{5.4b}$$

$$Si_2C(g) \leftrightarrow 2Si(g)+C(s) \tag{5.4c}$$

$$Si(g) \leftrightarrow Si(l) \tag{5.4d}$$

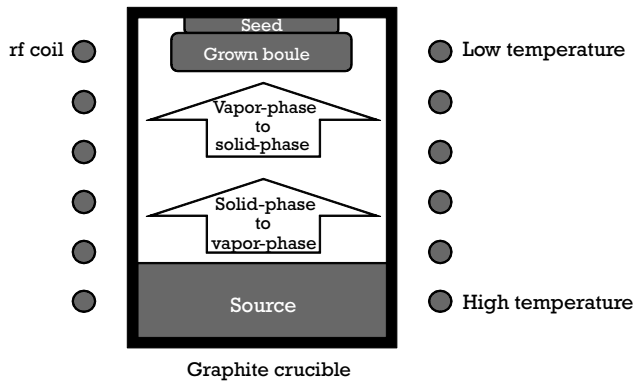

Figure 5.5 Schematic illustration of a crucible for seeded sublimation growth of SiC.

Due to the low stacking-fault energy of SiC (see Section 2.2.3), polytype mixing often occurs [34]. In the case of sublimation growth of heavily-nitrogen-doped n-type 4H-SiC ($000\overline{1}$) under optimized conditions, however, no polytype mixing occurs [35].

5.6.2 Doping During Sublimation Growth of SiC

SiC is doped with nitrogen by introducing nitrogen gas into the growth ambient. The incorporation of nitrogen in SiC crystal is determined by the equilibrium between nitrogen in the gas phase and nitrogen adsorbed on the growing surface [36]. Although nitrogen concentration N_N can be increased to 10^{20} cm^{-3}, N_N in commercial n-type 4H-SiC wafers is kept to less than 2×10^{19} cm^{-3} to suppress stacking-fault formation [37, 38].

P-type doping, on the other hand, is achieved by adding an aluminum-containing compound to the SiC source. The incorporation of aluminum into SiC crystal is almost proportional to the vapor pressure of aluminum in the crucible. However, heavy aluminum doping is still a challenge because it leads to preferential growth of 6H-SiC [35].

5.7 High-Temperature Chemical Vapor Deposition of SiC

High-temperature chemical vapor deposition (HT-CVD) has been developed to overcome the limitation of sublimation growth of SiC [39–41]. A SiC boule is grown at 2,400–2,700K and 0.2–0.7 atm in a vertical graphite crucible (Figure 5.6). Highly supersaturated vapor forms silicon and SiC clusters via homogeneous nucleation. Precursor gases (e.g., SiH_4 and C_3H_8 diluted in herium or H_2 carrier gas) are fed through a heating zone to a seed-crystal holder placed at the top of the reactor. The typical growth rate is 0.3–0.7 mm/h. Compared to sublimation growth, HT-CVD has the advantage that the supply of source material is maintained without depletion, thereby enabling growth of long SiC boules.

5.8 Solution Growth of SiC

As noted in Section 2.1, the solubility of carbon in silicon solution is very low. It, however, can be increased under high pressure. For instance, argon pressure of 98 atm was used for solution growth of SiC [42]; however, the SiC growth rate was below 0.5 mm/h around 2,500K.

The solubility of carbon in a silicon solution can also be increased by adding chromium, scandium, or titanium to a SiC solvent [43–49]. For instance, the maximum growth rate was reported to be 2 mm/h at 2,300K [49]; however, metallic contamination (in the order of 10^{17} cm^{-3} [50]) in the grown SiC could be a problem. With respect to doping, both p-type

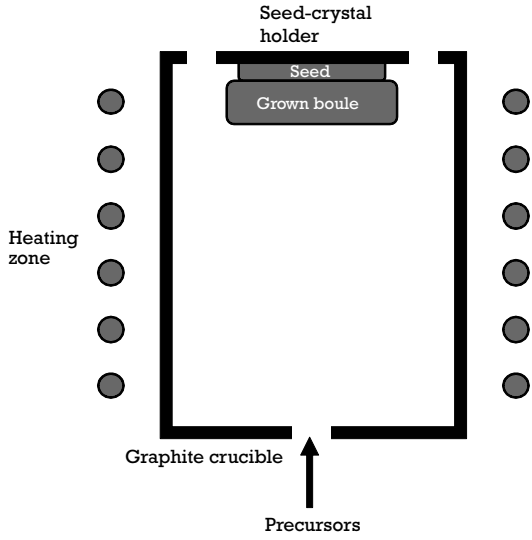

Figure 5.6 Schematic illustration of a reactor for HT-CVD of SiC.

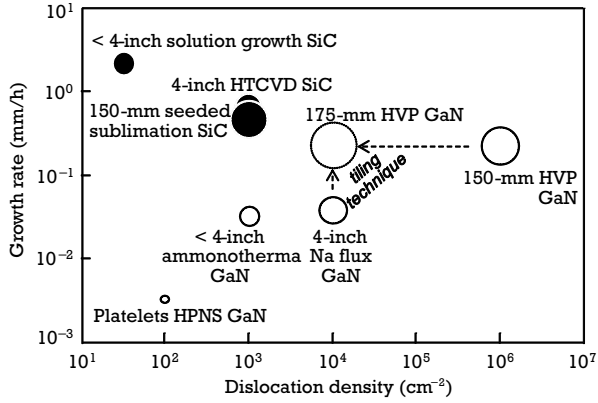

Figure 5.7 Comparison of reported growth rate and dislocation density of bulk GaN and 4H-SiC. The diameter of the circles schematically represents the reported maximum diameter of wafers.

and n-type 4H-SiC were successfully grown under Al-N codoping conditions [51].

5.9 Summary

Figure 5.7 compares the growth rate, dislocation density, and maximum wafer diameter of bulk GaN and 4H-SiC described in this chapter. A tiling

technique that merges multiple wafers grown by sodium-flux with a thick GaN layer by HVPE [14] is a candidate for fabricating large-area small-dislocation-density GaN wafers. As for 4H-SiC, seeded sublimation growth is possibly the most mature; however, solution growth is a candidate for high-quality 4H-SiC wafers.

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CHAPTER

6

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Epitaxial Growth

6.1 Introduction

Epitaxial growth is indispensable for fabricating designed layer structures in both GaN and 4H-SiC power devices (see Section 3.7). This chapter introduces the fundamentals of metal-organic chemical-vapor deposition (MOCVD) of GaN and chemical-vapor deposition (CVD) of 4H-SiC. In addition, the chapter introduces trench-filling epitaxial growth of 4H-SiC as an advanced technology for high-voltage 4H-SiC superjunction (SJ) power devices (see Chapters 8 and 9).

6.2 MOCVD of GaN

MOCVD (synonymously called metalorganic vapor-phase epitaxy [MOVPE], organometallic chemical-vapor deposition [OMCVD], or organometallic vapor-phase epitaxy [OMVPE]) has been the most dominant technique for epitaxial growth of III-V compound semiconductors [1]. The group III precursors used in the case of GaN-based materials are the same as

those used in the case of GaAs- and InP-based materials; namely, trimethylgallium (TMG), triethylgallium (TEG), trimethylaluminum (TMA), and trimethylindium (TMI). MOCVD of GaN-based materials differs from that of GaAs- and InP-based materials in terms of growth temperature due to the difference in the bond energies of group-V precursors; that is, a larger bond energy (about 400 kJ/mol) of ammonia (NH_3) compared to the bond energies (about 300 kJ/mol) of arsine (AsH_3) and phosphine (PH_3) [2, 3] requires a higher growth temperature (about 1,400K) for GaN-based materials compared that (about 1,200K) for GaAs- and InP-based materials.

An example of MOCVD system for epitaxial growth of GaN is schematically illustrated in Figure 6.1. Instead of TMG, TEG can be the metalorganic source. In the case of epitaxial growth of AlGaN and InGaN, TMA and TMI sources are also used. For n- and p-type doping, supply lines of n- and p-type dopant gases (e.g., silane [SiH_4] and biscyclopentadienyl magnesium [CP_2Mg]) are added, respectively, to the MOCVD system. Accurate control of the flow rates of these gases makes it possible to grow epitaxial layers of sophisticated devices.

MOCVD of GaN is usually carried out under a nitrogen-rich atmosphere. According to first-principles calculations and thermodynamic analysis, gallium is incorporated as gas-phase gallium atoms on the GaN growth surface, and the migration of these atoms is the rate-limiting process [4]. Experimentally, selective-area GaN MOCVD was used to separate areas with screw dislocations from those without screw dislocations [5]. Interstep distance λ_0 of a growth spiral (Figure 6.2) originating from a screw dislocation is given as [6].

$$\lambda_0 = 19\gamma V_m / m\Delta\mu \tag{6.1}$$

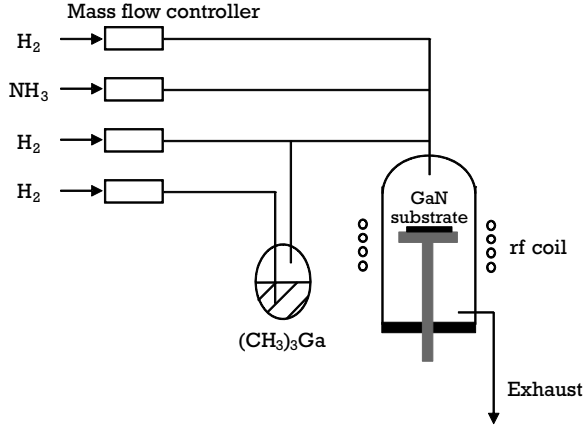


Figure 6.1 Schematic illustration of a GaN MOCVD system.

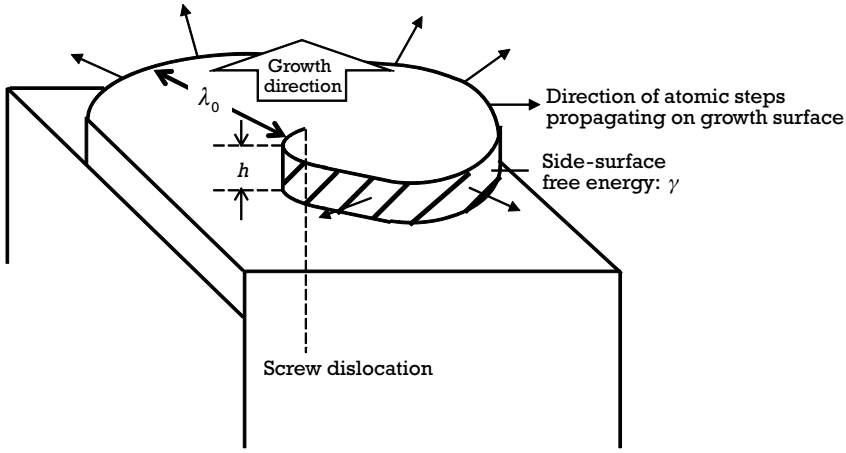


Figure 6.2 Schematic perspective view of a growth spiral originating from a screw dislocation. Narrow arrows show the direction of steps propagating on the growth surface (h: spiral-step height; γ: free energy of side surface of the spiral step).

where γ is the free energy of the side surface of the spiral step, V_m is the molar volume of the growing species, m is the number of spirals at the center (e.g., m =1 in Figure 6.3[a, b]; m = 2 in Figure 6.3[c]), and $\Delta\mu$ is the difference in the chemical potentials of the growth atmosphere and the crystal, given as [7].

$$\Delta\mu = RT \ln\alpha \tag{6.2}$$

where R is the ideal gas constant, T is the growth temperature, and α is the supersaturation ratio, defined as

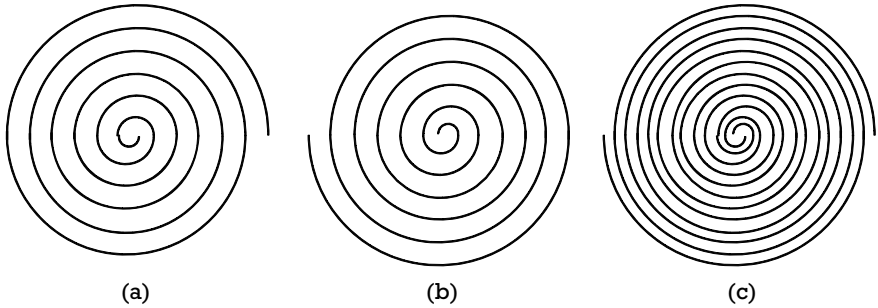


Figure 6.3 Schematic plan views of growth spirals originating from (a, b) one, and (c) two screw dislocations.

$$\alpha = \sigma + 1 \tag{6.3}$$

where σ is the supersaturation as defined in Section 5.2.1. As shown by the symbols in Figure 6.4, spiral- and nucleus-growth rates in areas, respectively, with and without screw dislocations during GaN MOCVD were plotted as a function of α (calculated from [6.1] and [6.2]) by Akasaka et al. [5] Their experimental results are reproduced by the dotted line calculated on the basis of the Burton–Cabrera–Frank (BCF) theory [8], which is described in Section 6.4. On the other hand, the growth rate in the case without screw dislocations is very low. This result means that α was lower than the critical supersaturation ratio α_{critical} for two-dimensional nucleation, which is explained in Section 6.3.

6.3 Two-Dimensional Nucleation Theory

Nucleation becomes dominant when α exceeds α_{critical}. This section introduces the expression for α_{critical} based on two-dimensional nucleation theory. The critical nucleation rate is expressed as [9]

$$J_{\text{nuc}} = Z\omega_{\text{nuc}} n_{\text{nuc}} \tag{6.3}$$

where Z is the Zeldovich nonequilibrium factor to account for depletion of the critical nuclei population due to their growth or decomposition, ω_{nuc} is

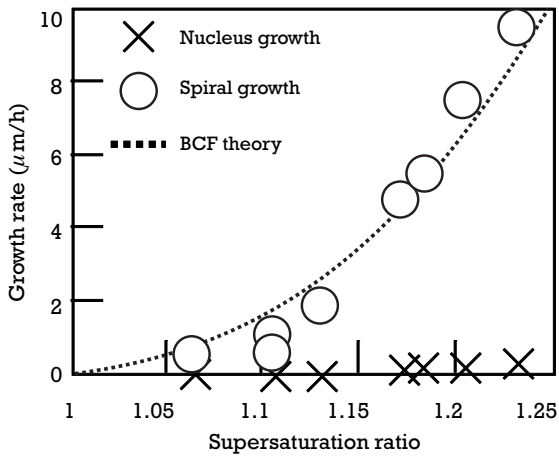


Figure 6.4 Experimental spiral-growth rate as a function of supersaturation ratio obtained by Akasaka et al. [5] (open symbols: experiments; dotted line: theoretical growth rate calculated on the basis of BCF theory) [8].

the frequency with which a nucleus grows to become supercritical, and n_{nuc} is the critical-nuclei concentration. Equation (6.3) can be rearranged as [9]

$$J_{nuc} = (2\pi r_{nuc} a \nu n_s n_0)\ (E_{nuc}/4\pi kTn_{nuc})^{0.5} \exp(-E_{diff}/kT) \exp(-E_{nuc}/kT)$$
$$\approx \exp(65) \exp(-E_{nuc}/kT) \quad (6.4)$$

where E_{nuc} is the free energy of nucleus formation, n_{nuc} and r_{nuc} are, respectively, the concentration and radius of atoms for a critical nucleus, a is the interatomic distance, ν is the atomic-vibration frequency, n_s is the sheet concentration of adatoms, n_0 is the sheet concentration of adatom sites, and E_{diff} is the activation energy for surface diffusion. In the case of a disk-shaped nucleus, E_{nuc} is expressed as [9]

$$E_{nuc} = \pi h_1 \gamma^2 \Omega/(kT \ln\alpha) \quad (6.5)$$

where h_1 is height of one Ga–N or Si–C bilayer (Figure 6.5), and is volume of an atom. Combining Equations (6.4) and (6.5) gives the well-known equation for $\alpha_{critical}$:

$$\alpha_{critical} = \exp\{\pi h_1 \gamma^2 \Omega/[(65 - \ln J_{nuc}) k^2 T^2]\} \quad (6.6)$$

6.4 BCF theory

BCF theory assumes that growth is conducted by steps provided from screw dislocations and that surface diffusion is the rate-limiting process [8]. It

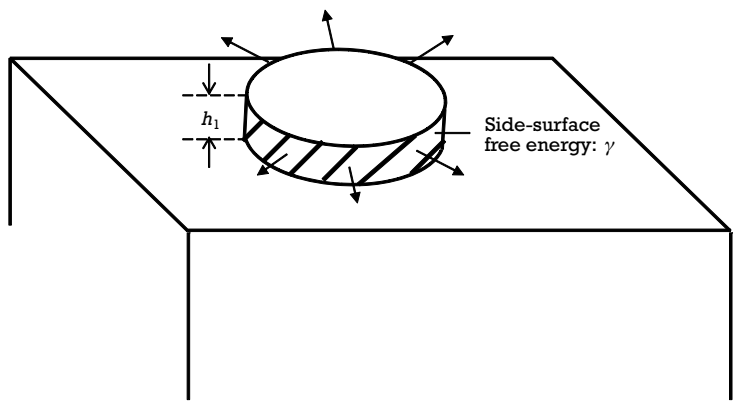


Figure 6.5 Schematic illustration of a two-dimensional nucleus with a height of one GaN or SiC bilayer and a side-surface free energy of γ. Arrows show the direction of steps propagating on the growth surface.

has been applied to vapor phase epitaxy of silicon [10, 11], GaAs under an arsenic-rich atmosphere [12], GaAs under a gallium-rich atmosphere [13], GaAsSb and InGaAs [14], 6H-SiC under a carbon-rich atmosphere [15], and 4H-SiC under a silicon-rich atmosphere [16]. In this section, a simple one-dimensional surface diffusion model based on BCF theory [8] is considered (Figure 6.6). During the diffusion of adatoms toward steps, some of the adatoms reach steps and are incorporated into the crystal, while others re-evaporate into the vapor.

When nucleation on terraces does not occur (i.e., $\alpha < \alpha_{\text{critical}}$—see Section 6.2), the net incoming flux onto the surface should be equal to the diffusion flux toward steps; namely,

$$-D_s(d^2n_s/dx^2) = J - n_s/\tau_s \tag{6.7}$$

where D_s and $n_s(x)$ are, respectively, the surface diffusivity and sheet concentration of adatoms, J is the incoming flux, and τ_s is the mean residence time of adatoms. If steps are assumed to be perfect sinks for adatoms (i.e., capture probability of adatoms at steps is unity), the boundary condition is expressed as

$$n_s(\pm\lambda_0/2) = n_{s0} \tag{6.8}$$

where n_{s0} is the equilibrium sheet-concentration of adatoms. The solution to (6.7) then becomes

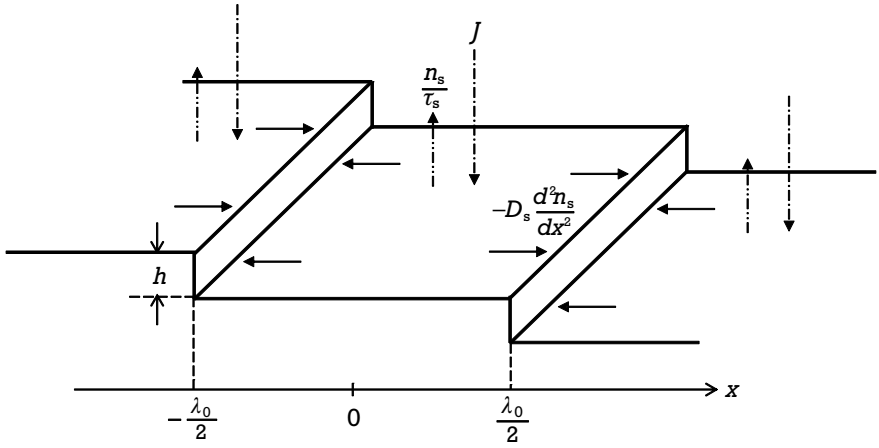


Figure 6.6 Schematic illustration of a spiral step treated one-dimensionally. Steps with height h are separated by equal distance λ_0.

$$n_s(x) = J\tau_s + (n_{s0} - J\tau_s)[\cosh(x/\lambda_s)/\cosh(\lambda_0/2\lambda_s)] \quad (6.9)$$

where λ_s is the surface diffusion length of adatoms, given as [8]

$$\lambda_s(x) = (D_s\tau_s)^{0.5} = a\exp[(E_{des} - E_{diff})/kT] \quad (6.10)$$

where E_{des} is the activation energy for desorption. Growth rate R_g is proportional to $(\sigma^2/\sigma_1)\tanh(\sigma_1/\sigma)$ [8], where

$$\sigma_1 = 9.5\gamma a/(mkT\lambda_s) \quad (6.11)$$

Namely, R_g is proportional to σ^2 (i.e., $[\alpha - 1]^2$) when $\sigma << \sigma_1$ (Figure 6.4), while R_g is proportional to σ (i.e., $\alpha - 1$) when $\sigma >> \sigma_1$.

When $\lambda_s >> \lambda_0$, $n_s(x)$ (6.9) becomes a parabola (Figure 6.7). When the flux of adatoms toward steps (i.e., $-D_s[dn_s/dx]$) is so small that maximum α at $x = 0$ is lower than $\alpha_{critical}$, two-dimensional nucleation on terraces does not occur. When $-D_s(dn_s/dx)$ becomes large enough for maximum α to exceed $\alpha_{critical}$, on the other hand, two-dimensional nucleation theory (Section 6.3) needs to be applied.

6.5 CVD of 4H-SiC

In CVD of SiC, silane (SiH_4) and propane (C_3H_8) are often used as precursors, and hydrogen (H_2) as a carrier gas. Growth temperature typically ranges from 1,800 to 1,950K. Since conventional cold-wall CVD reactors with horizontal [17] and vertical [18] configurations could not create a uniform temperature distribution, hot-wall CVD reactors have been developed [19]. In the case of hot-wall CVD reactors (Figures 6.8[a–c]), SiC wafers are placed inside gas-flow channels formed in susceptors, which are efficiently

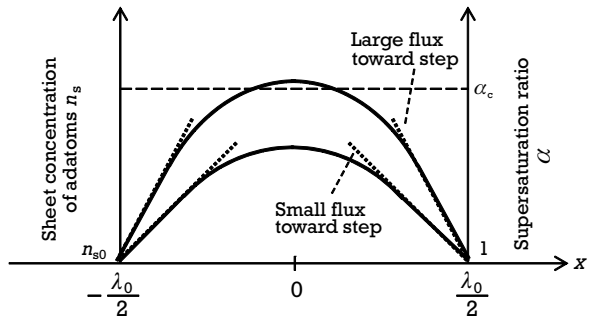


Figure 6.7 Distributions of $n_s(x)$ and $\alpha(x)$ when $\lambda_s >> \lambda_0$.

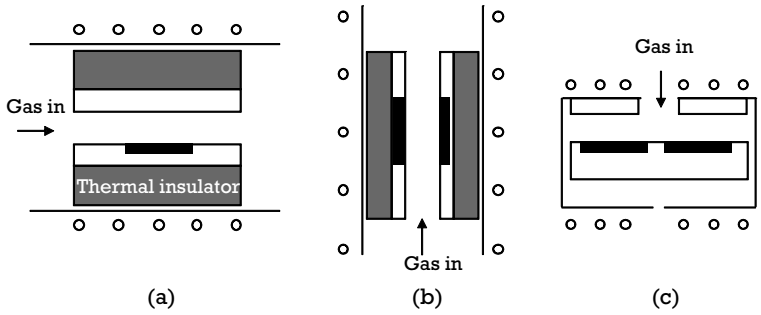


Figure 6.8 Schematic illustration of a SiC hot-wall CVD system: (a) horizontal, (b) chimney, and (c) planetary reactors.

heated by rf-induction. Since the wafers are heated by radiation from the front side and by conduction from the back side, temperature uniformity is easily established.

In the gas phase of SiC CVD, the major chemical reactions are considered as follows [20]:

$$SiH_4 \leftrightarrow SiH_2+H_2 \quad (6.12a)$$

$$Si_2H_6 \leftrightarrow SiH_2+SiH_4 \quad (6.12b)$$

$$SiH_2 \leftrightarrow Si+H_2 \quad (6.12c)$$

$$2H+H_2 \leftrightarrow 2H_2 \quad (6.12d)$$

$$C_3H_8 \leftrightarrow CH_3+C_2H_5 \quad (6.12e)$$

$$CH_4+H \leftrightarrow CH_3+H_2 \quad (6.12f)$$

$$C_2H_5+H \quad 2CH_3 \quad (6.12g)$$

$$2CH_3 \leftrightarrow C_2H_6 \quad (6.12h)$$

$$C_2H_4+H \leftrightarrow C_2H_5 \quad (6.12i)$$

$$C_2H_4 \leftrightarrow C_2H_2+H_2 \quad (6.12j)$$

$$H_3SiCH_3 \leftrightarrow SiH_2+CH_4 \quad (6.12k)$$

$$H_3SiCH_3 \leftrightarrow HSiCH_3+H_2 \quad (6.12l)$$

$$Si_2 \leftrightarrow 2Si \tag{6.12m}$$

$$Si_2+CH_4 \leftrightarrow Si_2C+2H_2 \tag{6.12n}$$

$$SiH_2+Si \leftrightarrow Si_2+H_2 \tag{6.12o}$$

$$CH_3+Si \leftrightarrow SiCH_2+H \tag{6.12p}$$

$$SiCH_2+SiH_2 \leftrightarrow Si_2C+2H_2 \tag{6.12q}$$

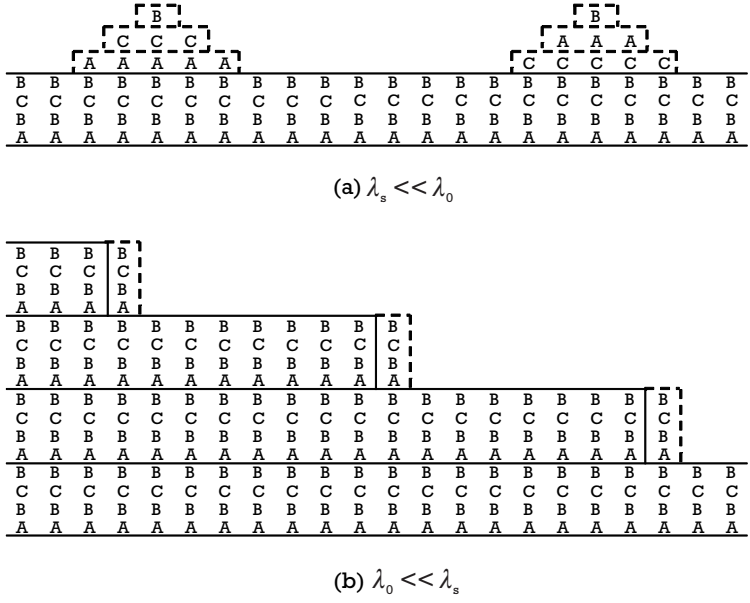
For n- and p-type doping, supply lines of n- and p-type dopant gases (e.g., nitrogen and TMA) are added, respectively. This section describes the fundamentals of 4H-SiC CVD. Section 6.6 introduces an advanced CVD technology for trench filling.

As described in Section 2.1, step-controlled epitaxy [21] for reproducing the same polytype of epitaxial layer as that of the substrate was proposed by Kuroda et al. In that study, the polytype of SiC layers on SiC (0001) substrates with various misorientations was investigated, and homoepitaxy of 6H-SiC was achieved. Moreover, homoepitaxial growth of 6H-SiC on misoriented 6H-SiC substrates was reported by Kong et al. [22, 23] In the case of 4H-SiC, homoepitaxial growth was similarly demonstrated [24].

It has been reported that steps appear on the surface of a misoriented substrate. Since these steps resemble spiral steps originating from a screw dislocation (Section 6.2), the two-dimensional nucleation theory (Section 6.3) and BCF theory (Section 6.4) can be similarly applied to deal with surface diffusion on the stepped surface of a misoriented substrate [10–16]. When $\lambda_s << \lambda_0$, crystal growth initially occurs on terraces through two-dimensional nucleation (Figure 6.9[a]). As described in Section 2.2.2, the polytype, which is mainly determined by growth temperature, will become 3C under that condition. As a result, 3C-SiC grows with two stacking orders, namely, ABCABC… and ACBACB… When $\lambda_s >> \lambda_0$, on the other hand, adatoms migrate and reach steps (Figure 6.9[b]). The dominant steps of misoriented 4H-SiC (0001) are two or four bilayers high [25], leading to unique determination of incorporation sites A, B, and C at the steps and replication of the substrate polytype in the epitaxial layer.

According to a simulation of surface mass fluxes in the SiH_4–C_3H_8–H_2 growth system [17, 26], the surface reaction of silicon adatoms with acetylene (C_2H_2), namely,

$$2Si+C_2H_2 \leftrightarrow 2SiC+H_2 \tag{6.13}$$



(a) $\lambda_s << \lambda_0$

(b) $\lambda_0 << \lambda_s$

Figure 6.9 Schematic illustration of occupation sites (A, B, and C) in the hexagonal close-packed structure of epitaxial layers grown on surfaces when (a) $\lambda_s << \lambda_0$ and (b) $\lambda_s >> \lambda_0$ in the cases of terraces and four-bilayer steps.

is one of the most active surface reactions involved. Based on (6.13), the surface diffusion of silicon adatoms under a carbon-rich atmosphere was analyzed using two-dimensional-nucleation (Section 6.3) and BCF (Section 6.4) theories by Kimoto and Matsunami [15]. However, in that analysis, the free energy of (0001) surfaces was incorrectly applied to the side surface of a two-dimensional nucleus. Therefore, in the following, surface diffusion of C_2H_2 molecules under a silicon-rich atmosphere [16] is analyzed.

4H-SiC on 4H-SiC (0001) substrates with an off angle θ of 1°–45° were grown in a SiH_4 (1.5–2.0 sccm)–C_3H_8–H_2 (8.0 slm)–argon (0.8 slm) system under a silicon-rich atmosphere (i.e, C/Si ratio [atomic ratio of carbon to silicon] of 0.5–0.75) at T = 1,773K and growth pressure of 80 Torr by Saito and Kimoto [27]. Here sccm denotes standard cubic centimeters per minute, and slm denotes standard liters per minute. In step-flow growth mode, where nucleation on terraces does not occur (Section 6.4), the net flux of C_2H_2 molecules onto the surface is equal to the diffusion flux toward steps. From (6.9), which is the solution to the continuity equation (6.7), the flux of C_2H_2 in the x direction, $J_s(x)$, is obtained as

$$J_s(x) = -D_s(dn_s/dx) = \lambda_s[J-(n_{s0}/\tau_s)][\sinh(x/\lambda_s)/\cosh(\lambda_0/2\lambda_s)] \qquad (6.14)$$

The step velocity is calculated by assuming C_2H_2 molecules diffuse from the left and right sides of the steps. Since two carbon atoms are provided by one C_2H_2 molecule at the step edges [14], R_g is given by the product of the step velocity and tan θ (i.e., h/λ_0) as [15]

$$R_g = (4h\lambda_s / n_0\lambda_0)\ [J-(n_{s0}/\tau_s)]\tanh(\lambda_0/2\lambda_s) \tag{6.15}$$

When $\lambda_s >> \lambda_0/2$, R_g becomes independent of λ_0 {i.e., $(2h/n_0)$ $[J-(n_{s0}/\tau_s)]$}. According to [27], R_g depends little on θ when $\theta = 4°–45°$, but it decreases when $\theta = 1°$. λ_s is thus estimated to be comparable to or less than $h/(2\tan 1°)$ (i.e., 14.4 nm for two-bilayer-high steps and 28.9 nm for four-bilayer-high steps). If n_0 is assumed to be equal to the concentration of sites of silicon adatoms on the surface (1.21×10^{15} cm^{-3}), $J-(n_{s0}/\tau_s)$ can be calculated from (6.15). Dependences of $J-(n_{s0}/\tau_s)$ on the C/Si ratio calculated from (6.15) for λ_s of 12–36 nm are shown in Figure 6.10. When λ_s = 12–18 nm in the case of two-bilayer-high steps and λ_s = 24–36 nm in the case of four-bilayer-high steps, the least-squares fit of $J-(n_{s0}/\tau_s)$ matches those of

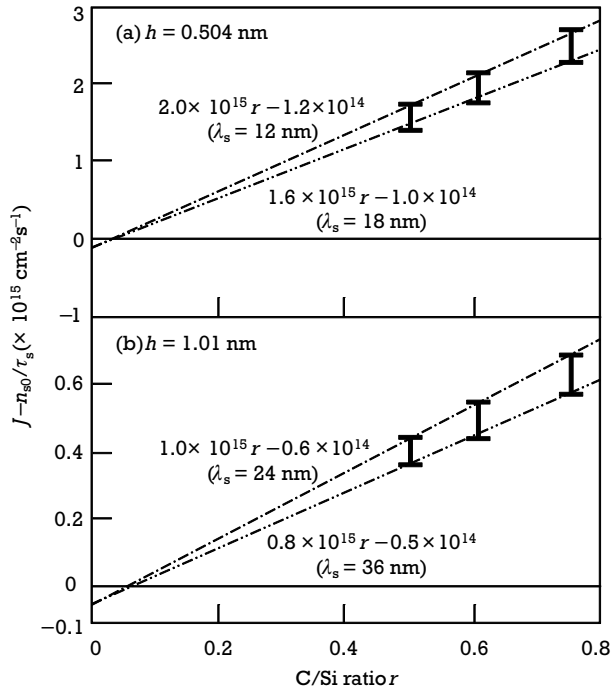


Figure 6.10 Dependences of $J-(n_{s0}/\tau_s)$ on the C/Si ratio calculated from (6.15) for λ_s of 12–36 nm. Experimental results denoted by error bars are taken from [27]. Lines and corresponding equations show the least-squares fit to the experimental results.

$\theta = 1° - 45°$. This λ_s range agrees with the above estimated values (i.e., 14.4 and 28.9 nm). The absolute value of the intercept with the vertical axes in Figure 6.10(a, b) give an equilibrium desorption flux of C_2H_2 molecules, n_{s0}/τ_s, of (0.5–1.2) × 10^{14} $cm^{-2}s^{-1}$. This value corresponds to the equilibrium vapor pressure of C_2H_2 molecules ($P_{C_2H_2}^{e}$) of (0.4–1.0) × 10^{-4} Pa, which is obtained from Knudsen's equation [14], namely,

$$n_{s0}/\tau_s = P_{C_2H_2}^{e}/(2\pi m_{C_2H_2} kT)^{0.5} \tag{6.16}$$

where $m_{C_2H_2}$ is the mass of a C_2H_2 molecule.

In two-dimensional nucleation mode, where nucleation on terraces occurs (Section 6.3), under a silicon-rich atmosphere, the equilibrium vapor pressure of silicon adatoms must be similar to the incoming pressure of silicon; namely, the supersaturation ratio for silicon (α_{Si}) equals unity [12]. Since the supersaturation ratio for carbon (α_C) reaches a maximum at the center of a terrace (i.e., $x = 0$) (Figure 6.7), the maximum supersaturation ratio for SiC is obtained from (6.9) as

$$\alpha_{max} \equiv \alpha_{Si}\,\alpha_C(x=0) \approx 1+(\lambda_0 n_0 R_g/4h\lambda_s)(\tau_s/n_{s0})\tanh(\lambda_0/4\lambda_s) \tag{6.17}$$

Nucleation on terraces becomes dominant when α_{max} exceeds $\alpha_{critical}$ (see Section 6.3). For a disk-shaped nucleation per second on a 10×10-nm^2 area, (6.6) becomes

$$\alpha_{critical} = \exp\{\pi h_1 \gamma^2 \Omega/[(65-\ln 10^{12})k^2T^2]\} \tag{6.18}$$

where h_1 is height of one Si-C layer (0.252 nm) and Ω is the volume of the Si-C pair (2.07 × 10^{-23} cm^3). The free energy of the side surface of a two-dimensional nucleus under a silicon-rich atmosphere is assumed to be 2.22 J/m^2, which is the calculated γ for silicon-terminated 3C-SiC (111) [28]. From (6.17) and (6.18), the off-angle dependence of critical growth rate (R_c) for mode transition between step-flow growth and two-dimensional nucleation is calculated at T = 1,773K (Figure 6.11). It is confirmed that the range of R_c, originating from variation in determining λ_s (Figure 6.10), does not depend on h (h = 0.504 or 1.01 nm). It is also confirmed that the experimental data for step-flow growth in [27] are in the bottom-right region under the curve calculated using n_{s0}/τ_s and λ_s values obtained from Figure 6.10.

According to (6.17), R_c increases with increasing n_{s0}/τ_s. According to (6.13) and (6.16), an increase in n_{s0}/τ_s, namely, an increase in $P_{C_2H_2}^{e}$, is achieved by reducing the SiH_4 flow rate. To maintain the C/Si ratio at less than unity (i.e., a silicon-rich atmosphere), however, the C_3H_8 flow rate

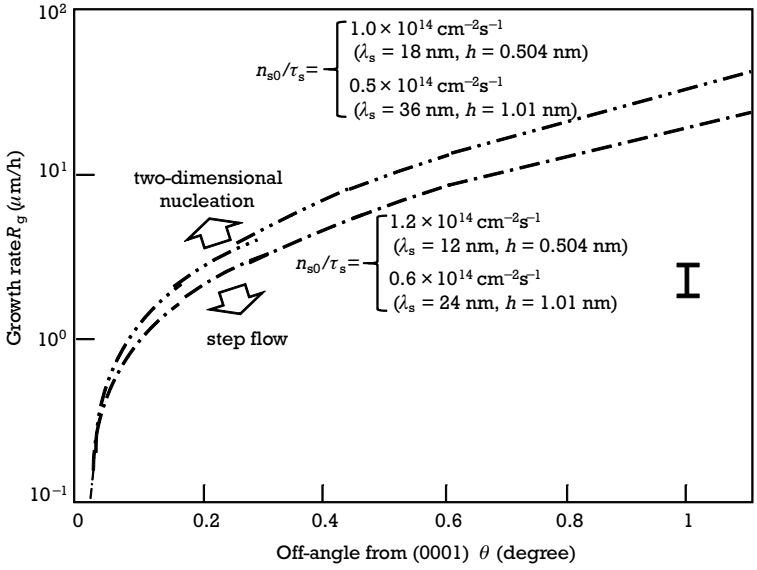


Figure 6.11 Off-angle dependence of the critical growth rate for mode transition between step-flow growth (bottom-right region) and two-dimensional nucleation (top-left region) calculated with the equilibrium desorption flux and surface diffusion length of C_2H_2 molecules obtained from Figure 6.10. Data denoted by an error bar is taken from [27].

must be limited, resulting in a lower R_c. The calculated curves in Figure 6.11 are thus considered to be close to the practical limit at T = 1,773K.

6.6 CVD Trench Filling of 4H-SiC

As shown in Figure 2.18, the breakdown voltage (BV) of a p$^+$n junction with an n-type drift layer is equal to $E_{critical}W_D/2$ (Figure 6.12[a] and the dashed line in Figure 6.12[c]). In the case of a p$^+$n junction with alternating n- and p-type regions within a drift layer (a so-called SJ diode) [29], the same BV can be realized with a drift layer with half the thickness (i.e., $W_D/2$) (Figure 6.12[b] and the solid line in Figure 6.12[c]) because N_D in (2.2) becomes effectively zero. SJ structures thus improve the trade-off relationship between BV and specific resistance of the ideal drift layer R_{ideal} (Section 2.7). The first 4H-SiC SJ diode with BV = 1.5 kV was fabricated by multiepitaxy [30], by which multiple n-type epitaxial layers are grown over patterned ion implanted p-type regions to create alternating p/n columns. In the case of a silicon SJ structure, the p-type regions merge due to controlled diffusion of p-type dopant (i.e., boron) during epitaxial growth [31]. However, this diffusion is not feasible in a SiC SJ structure due to the very low diffusivity of aluminum or very large diffusivity of boron [30]. Refilling

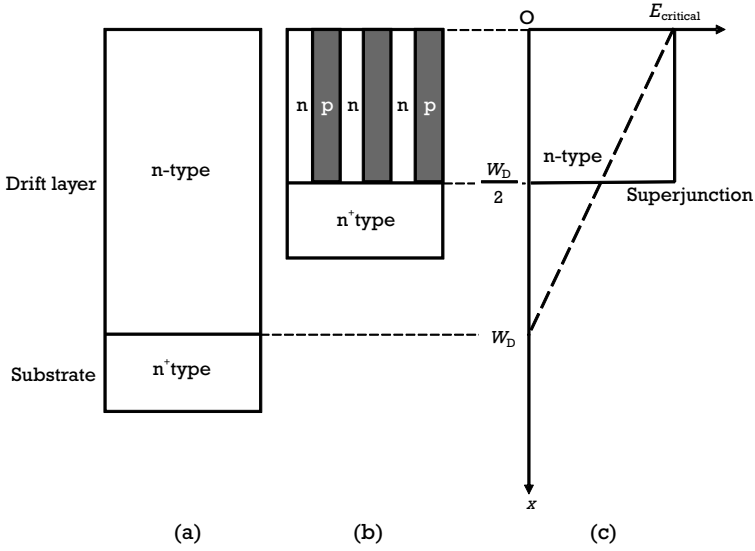


Figure 6.12 Drift layers consisting of (a) an n-type semiconductor and (b) a superjunction structure, together with (c) their electric-field distributions.

an epitaxial layer into 4H-SiC trenches is therefore highly practicable for 4H-SiC SJ power devices with $BV > 2$ kV [32, 33].

In a conventional SiH_4:C_3H_8:H_2 CVD system [33–37], the use of a relatively high pressure (up to 38 kPa [38]) reduces the mean free path of growing species comparable to the size of microtrenches, thereby allowing the continuous-fluid approximation to be used [39]. In the case of a large growth rate on a bare wafer (R_0), the isoconcentration contours of growing species close to a nonplanar surface are parallel to the surface, as shown by the dotted lines in Figure 6.13(a). Fluxes toward the mesa top and the trench bottom, respectively, become large and small, resulting in morphological instability. When R_0 is small (e.g., due to re-evaporation of growing species at a relatively high temperature [1,923K] [33]) and the radius of curvature (r) is small, the shape of the isoconcentration contours changes due to the two-dimensional Gibbs–Thomson effect [40, 41], namely,

$$C^e(r) = C^e(\infty) \exp[\gamma V_m / RTr] \tag{6.19}$$

where $C^e(r)$ is the equilibrium gas-phase concentration of the growing species in contact with a curved surface with radius r (Figure 6.13[b]). Note that the sign of r depends on whether the mesa surface is convex upward ($r > 0$) or convex downward ($r < 0$). Note also that (6.19) becomes

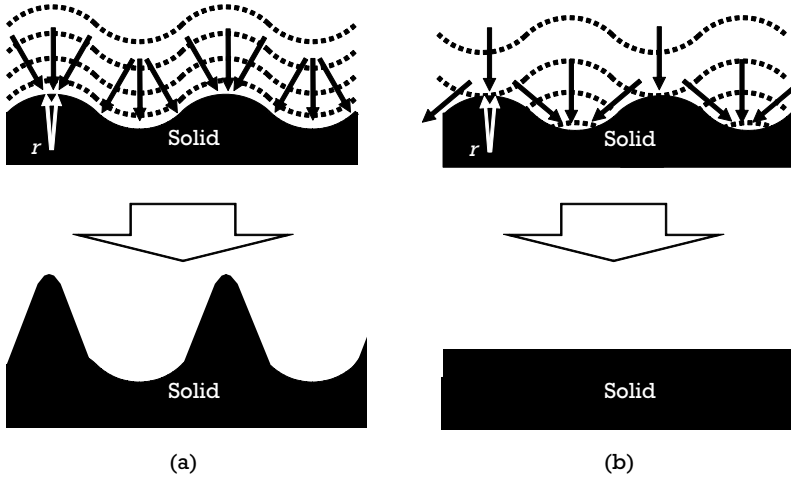


Figure 6.13 Schematic cross sections of nonplanar growing surfaces when the growth rate and radius of curvature (r) are (a) large and (b) small. Dotted lines and solid arrows, respectively, show isoconcentration contours and direction of fluxes of growing species in the vapor.

$$C^{e}(r) = C^{e}(\infty)\exp[2\gamma V_{m}/RTr] \tag{6.20}$$

under the three-dimensional Gibbs–Thomson effect [42].

To further reduce R_0, hydrogen chloride (HCl) gas has been added to the procedure for conventional CVD growth [43–45]. The resultant fluxes toward the mesa top and the trench bottom, respectively, become small and large, resulting in a uniform surface. In the case of shallow (< 5 μm-deep) trenches, dependences of experimentally measured growth rates (both at the mesa top and on the trench bottom) on trench pitch were reproduced with (6.19) [41, 46]. Experimentally, by overcoming the strong impact of slight misalignment of trench-direction from the $[11\bar{2}0]$ direction, 25-μm-deep n-type 4H-SiC trenches were refilled with p-type 4H-SiC [47].

6.7 Summary

This chapter explains the fundamentals of GaN MOCVD and 4H-SiC CVD on the basis of the two-dimensional nucleation and BCF theories. In addition, the chapter explains the trench-filling epitaxial growth of 4H-SiC as an advanced technology for fabricating SJ structures. To apply this trench filling to 4H-SiC SJ power devices, however, developing techniques for evaluating distribution of p-type dopant is considered indispensable.

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CHAPTER

7

Contents

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7.2 Etching

7.3 Ion Implantation

7.4 Diffusion

7.5 Oxidation

7.6 Metallization

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7.8 Summary

Fabrication Processes

7.1 Introduction

This chapter introduces the basic aspects of the processing steps for fabricating GaN and 4H-SiC power devices, excluding epitaxial growth (already described in Chapter 6). Sections 7.3 and 7.4 describing, respectively, ion implantation and diffusion, cover mainly topics associated with 4H-SiC. Sections 7.2 and 7.5– 7.7, dealing, respectively, with etching, oxidation, metallization, and passivation comparatively describe GaN and 4H-SiC device processing.

7.2 Etching

Since both GaN and 4H-SiC are extremely inert materials in regard to conventional wet chemical etching, they are usually etched with a high-density plasma, such as magnetron reactive ions, an electron-cyclotron-resonance plasma, or an inductively coupled plasma (ICP). Among these techniques, ICP etching achieves the highest etching rate; for example, the first ICP etching of GaN in a chlorine/hydrogen/argon

plasma resulted in an etching rate of about 0.7 μm/min [1, 2]. ICP plasmas are formed by an inductive coil to which RF (radio frequency) power is applied (Figure 7.1). Ion energy and plasma density can be decoupled, resulting in uniform density and energy distributions, even with low ion and electron energies. Consequently, ICP etching can produce low damage while maintaining a high etching rate. Anisotropic etching is achieved by applying an RF bias to the samples being etched. This section describes ICP etching and wet chemical etching of GaN and 4H-SiC in terms of reported results.

7.2.1 ICP Etching

Halogen- and methane-based ICP plasmas have been used for ICP etching of GaN [3–8]. For halogen-based plasmas, etch rates are limited by the volatility of the group-III halogen etch product. Among halogen-based plasmas, chlorine-based plasmas typically yield high etching rate. For methane-based plasmas, on the other hand, the etching rate is much lower. Although these techniques for ICP etching can minimize plasma damage, their influence on device characteristics cannot be neglected. According to Ohta et al., the damage was removed by thermal treatment at 850°C [9].

For the ICP etching of SiC, fluorine-, chlorine-, and bromine-based plasmas have been used [10–14]. Fabrication of 25-μm-deep 4H-SiC trenches has also been demonstrated [15] for superjunction structures (Chapters 6, 8, and 9).

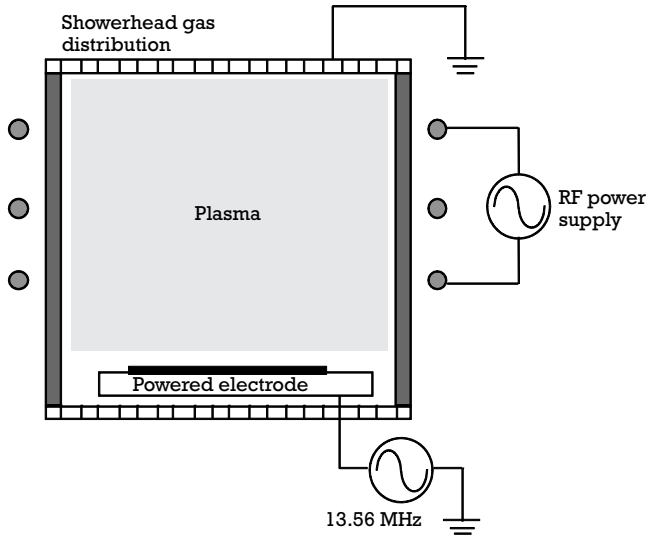

Figure 7.1 Schematic illustration of an ICP etcher.

7.2.2 Wet Chemical Etching

Wet chemical etching of semiconductors in general involves oxidation of the semiconductor surface and subsequent dissolution of the resulting oxides. Oxidation requires holes that can be supplied either chemically or via an electrochemical circuit [16].

7.2.2.1 Chemical Eching

With respect to the chemical etching of GaN, gallium- and nitrogen-polar surfaces reportedly showed different etching characteristics; that is, only nitrogen-polar surfaces (of both epitaxial GaN layers [17] and bulk GaN [18]) were etched in aqueous KOH. The mechanism of etching a nitrogen-polar GaN surface was interpreted as [19]

$$2GaN+3H_2O \rightarrow Ga_2O_3+2NH_3 \tag{7.1}$$

where KOH works as a catalyst and a solvent for Ga_2O_3. Unlike a nitrogen-polar surface, a gallium-polar (0001) surface is selectively attacked and shows hexagonal etch pits in hot (470–490K) phosphoric acid [20–24].

With respect to the chemical etching of SiC, on the other hand, etching in phosphoric acid is impractical because of the low etching rate. Instead, molten KOH has been used to oxidize SiC and remove the formed oxide [25]. However, contamination of potassium must be avoided, especially during SiC oxidation [26]. Moreover, care must be taken to create dislocation pits because the KOH-etching rate becomes higher around the intersection points of dislocations with a surface.

As for wet etching after trench structures have been fabricated, the use of 25% tetramethylammonium hydride (TMAH) at 358K was reportedly effective for obtaining smooth GaN $(1\bar{1}00)$ planes [27]. TMAH is widely used in lithography as a basic solvent in the development of an acidic photoresist and is free from the contamination by alkaline metal.

7.2.2.2 Photoelectrochemical Etching

Photoelectrochemical etching (PEC) is independent of crystal polarity of GaN [28]. The first PEC etching of GaN used a He-Cd laser (with a wavelength of 325 nm) in an aqueous KOH solution (with an etching rate of 400 nm/min) or in an aqueous HCl solution (with an etch rate of 40 nm/min) [29]. PEC etching has also been used in the case of AlGaN/GaN heterostructures. For example, in the case of $Al_{0.2}Ga_{0.8}N$/GaN heterojunction field-effect transistors, wet gate-recess etching using a 35-mW/cm^2 mercury arc lamp and 0.5-mol% KOH was demonstrated. In that demon-

stration, a DC bias of 2V was applied between the mesa-etched surface of the edge region of a two-inch wafer and the platinum grid (Figure 7.2) [30].

In the case of a SiC p-n junction, p-type SiC can be selectively etched without ultraviolet light illumination because of the lack of holes in n-type SiC [31, 32]. Etching of n-type SiC, on the other hand, is possible under the illumination of ultraviolet light with above-bandgap photons [33–37]. Photogenerated holes are accumulated at the electrolyte (e.g., KOH solution)/n-type SiC interface, while holes are depleted at the electrolyte/p-type SiC interface.

7.3 Ion Implantation

As described in Sections 3.1 and 3.7, GaN and 4H-SiC power devices are often made from n-type starting material, and the use of p-type dopant implantations for active regions is avoided in the case of p^+n diodes. In the case of unipolar power devices, on the other hand, aluminum-ion implantation into 4H-SiC is frequently used; however, magnesium-ion implantation into GaN is not much used because of a very low activation ratio (Section 3.7). Boron-ion implantation into 4H-SiC is not much used either, for the following reason. An energetic ion penetrating through a 4H-SiC (or GaN) crystal generates a collision cascade consisting of silicon vacancies V_{Si} and carbon vacancies V_C (or gallium vacancies V_{Ga} and nitrogen vacancies V_N) as well as silicon interstitials I_{Si} and carbon interstitials I_C (or gallium interstitials I_{Ga} and nitrogen interstitials I_N). Post-implantation annealing is

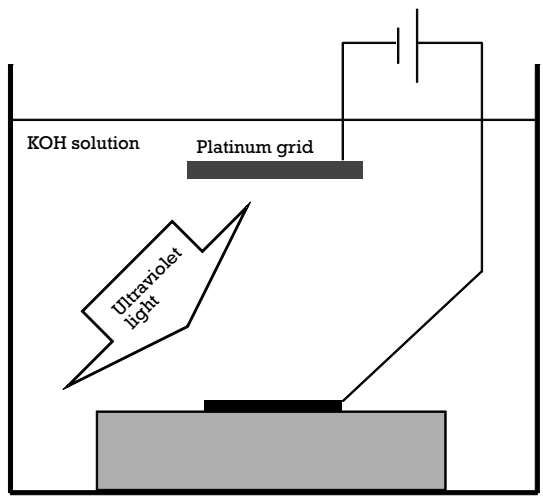

Figure 7.2 Schematic illustration of a PEC etching apparatus used for etching an AlGaN/GaN heterostructure [30].

thus needed, and redistribution of boron in SiC during annealing becomes very large (Sections 6.6 and Section 7.4).

During post-implantation annealing, surface degradation occurs. A SiN cap is conveniently used for post-implantation annealing of implanted GaN around about 1,500K [38]. In the case of SiC, on the other hand, a carbon cap is frequently employed for post-implantation annealing around 1,950K [39].

As for n-type dopant implantations, silicon-ion implantation into GaN and nitrogen-ion and phosphorus-ion implantations in 4H-SiC have been frequently used.

7.3.1 Ion Implantation into GaN

Magnesium-ion implantation has been attempted using a high-quality n-type GaN epitaxial layer grown on a freestanding GaN substrate, and p-type conversion was confirmed by the following three experimental results [40].

1. Low-temperature photoluminescence spectra of the layer showed magnesium-acceptor related emissions.
2. Vertical diodes showed clear rectifying *I-V* characteristics and emitted ultraviolet and blue-green light when forward-biased.
3. Positive Hall coefficients were also observed. However, increasing the activation ratio of magnesium acceptors is still a challenge.

Silicon-ion implantation has been used for fabricating AlGaN/GaN high-electron mobility transistors (HEMTs) [41] to reduce metal/GaN contact resistance and fabricate a lightly doped channel region. It has also been applied to p-type GaN to fabricate normally-off GaN metal-insulator-semiconductor field-effect transistors (MISFETs) with a threshold voltage of +3.4V [42].

7.3.2 Aluminum-Ion Implantation into 4H-SiC

In the case of boron-ion implantation into silicon, scatter-in channeling [43] (or so-called paradoxical profile broadening [44]) was observed during high-tilt-angle implantation (e.g., 7° for [100] Si) through a randomized surface layer. In the scatter-in process, some high-energy ions, which move in a random direction after crossing the surface layer, are scattered in channeling directions and penetrate deeper into the undamaged underlying crystal. When the tilt angle is 0°, the depth of the as-implanted profile decreases with the increasing thickness of the surface oxide because a well-collimated ion beam is scattered by the amorphous oxide layer (i.e.,

amorphization-suppressed channeling). On the other hand, at higher tilt angles and at certain energies, the as-implanted profile becomes deeper with increasing oxide thickness because of scatter-in channeling [45].

In the case of aluminum-ion implantation into 4H-SiC, the substrate is usually misoriented from (0001) by 4°–8° to achieve step-flow epitaxial growth [46]. Thus, scatter-in channeling of aluminum has such a high probability that the effect of a surface oxide on channeling becomes important. Moreover, due to the negligible diffusivity of aluminum in 4H-SiC, multiple-energy aluminum implantations have to be used to form box-like profiles. The sequence of implantations (i.e., increasing or decreasing order of implantation energy) is thus important in determining whether the scatter-in channeling or amorphization-suppressed channeling dominates the box-like profiles. Mochizuki et al. used a 4H-SiC wafer (misoriented by 8° from (0001) toward [$11\bar{2}0$]) with and without a 35-nm-thick SiO_2 layer for five-fold aluminum implantation at room temperature to achieve 0.3-μm-deep boxlike profiles with a mean plateau concentration of 1×10^{19} cm^{-3} [47]. Implantation energies (keV) and corresponding doses ($\times 10^{13}$ cm^{-2}) were 220/10, 160/5, 110/7, 70/6, and 35/3. The implantation without the SiO_2 layer in a decreasing energy order resulted in the least-extended tail in the aluminum-concentration profiles. The tail of the profiles for implantation with the SiO_2 layer extends deeper than that for implantation without the SiO_2 layer. This difference resulted from the scatter-in channeling. In the case of increasing order of implantation energy, on the other hand, little difference between the tails of the profiles for implantations with and without the SiO_2 layer was observed. Thus, the effect of amorphization-suppressed channeling was less than that of scatter-in channeling.

To analytically express a wide selection of implanted ion profiles in 4H-SiC, Pearson frequency distribution functions [48] have been successfully applied [49]. For heavy ions such as aluminum, however, large channeling tails of distributions deviate from the single-Pearson distribution functions [49–51]. The dual-Pearson distribution, which is a weighted sum of two Pearson distribution functions [48], has thus been used to model the randomly scattered portion and the channeled portion of the profile [52]. The depth profile of aluminum, $N(x)$, is represented by

$$N(\mathrm{x}) = D_1 f_1(x) + D_2 f_2(x) \tag{7.2}$$

$$f_i(x) = K_i[1+\{(x-R_{\mathrm{p}i})/A_i - n_i/r_i\}^2]^{-\mathrm{m}_i} \exp[-n_i \arctan\{(x-R_{\mathrm{p}i})/A_i - n_i/r_i\}^2] \quad (i = 1, 2) \tag{7.3}$$

where f_1 and f_2 are, respectively, normalized Pearson type IV distribution functions for the randomly scattered and channeled components of the

profile, and D_1 and D_2 are the doses represented by each Pearson function. For Pearson type IV distribution functions, K_1 and K_2 are normalized constants. R_{p1} and R_{p2} are projected ranges, and n_1, n_2, r_1, r_2, A_1, A_2, m_1, and m_2 are parameters related to the range stragglings ΔR_{p1} and ΔR_{p2}, skewnesses γ_1 and γ_2, and kurtoses β_1 and β_2, as follows:

$$r_i = -(2+1/b_{2i}) \tag{7.4a}$$

$$n_i = -r_i b_{1i}/(4b_{0i}b_{2i}-b_{1i}^2)^{0.5} \tag{7.4b}$$

$$m_i = -1/(2b_{2i}) \tag{7.4c}$$

$$A_i = m_i r_i b_{1i}/n_i \tag{7.4d}$$

$$b_{0i} = -\Delta R_{pi}^2(4\beta_i-3\gamma_i^2)C \tag{7.4e}$$

$$b_{1i} = -\gamma_i\Delta R_{pi}(\beta_i+3)C \tag{7.4f}$$

$$b_{2i} = -(2\beta_i-3\gamma_i^2-6)C \tag{7.4g}$$

$$C = 1/[2(5\beta_i-6\gamma_i^2-9)]\ (i = 1, 2) \tag{7.4h}$$

Dose ratio R is defined as

$$R = D_1/(D_1+D_2) \tag{7.5}$$

To avoid arbitrariness of R_{p2} [53], R_{p2} was set equal to R_{p1} (Figure 7.3).

Comparing the dual-Pearson parameters with the single-Pearson parameters shows that the dependences of R_p in the case of implantation without the SiO_2 layer, ΔR_{p1}, and γ_1 are almost the same as those stated in two reports [49, 50], but they slightly differ from those stated in another report [51]. Although β values of the reported single-Pearson model are not shown to avoid complexity, the obtained relationship between β_1 and r_1 in Figure 7.3(e),

$$\beta_1 = 1.19\beta_{1o} \tag{7.6a}$$

$$\beta_{1o} = [39\gamma_1^2+48+6(\gamma_1^2+4)^{1.5}]/(32-\gamma_1^2) \tag{7.6b}$$

is very similar to the following reported relationship [51]:

$$\beta = 1.30\beta_o \tag{7.6c}$$

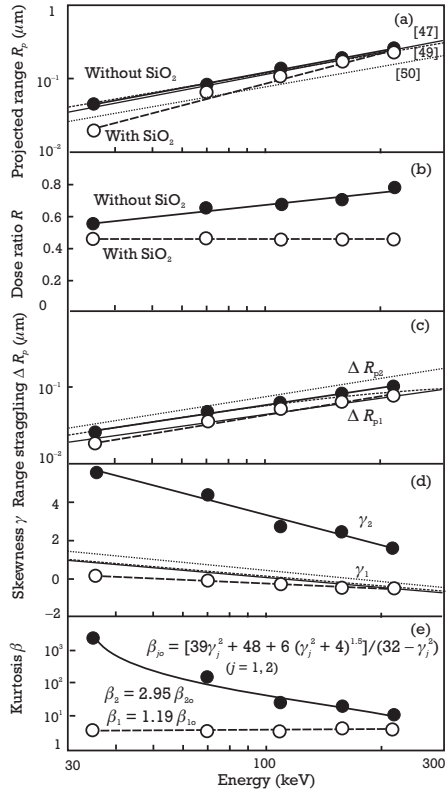

Figure 7.3 Dual-Pearson parameters as a function of implantation energy. (Projected ranges, range stragglings, and skewnesses from previous reports are also shown for comparison.)

In Figure 7.3(a), R_p for implantations with the SiO_2 layer is smaller than that for implantations without the SiO_2 layer. This result is due to the existence of the SiO_2 layer during implantation. On the other hand, in Figure 7.3(b), compared to R for implantations without the SiO_2 layer, R for implantations with the SiO_2 layer becomes smaller, (i.e., more aluminum ions channel, owing to the scatter-in channeling). It should be noted that in the case of aluminum implantations with the 35-nm-thick SiO_2 layer, R monotonically increases under the following conditions [54]:

- Dose of 1×10^{14} cm^{-2} and energy exceeding 300 keV;
- Dose of 1×10^{15} cm^{-2} or more and energy of 35 keV or more.

This result suggests that under either condition, the influence of the amorphization-suppressed channeling [43] might also increase.

Lateral range straggling can be extracted by expressing the lateral-concentration profiles as a one-dimensional dual-Pearson-distribution function multiplied by another distribution function (e.g., a Gaussian function). Such a two-dimensional model should contribute to efficiently simulating the current-voltage characteristics of 4H-SiC power devices [55, 56]. In addition to the dual-Pearson approach, Monte-Carlo simulation using binary-collision approximation (BCA) [57, 58] has also been used. Asymmetric lateral straggling due to a surface misorientation of a SiC substrate was shown with BCA simulation [59].

7.3.3 Nitrogen-Ion and Phosphorus-Ion Implantations into 4H-SiC

Concentration profiles of implanted nitrogen and phosphorus ions have been analyzed by taking a single-Pearson approach [49, 60–62]. In Figure 7.4, obtained R_p and ΔR_p are shown as a function of implantation energy in nitrogen and phosphorus ion implantation into SiC. Both nitrogen and phosphorus atoms show negligible diffusion during post-implantation annealing [63].

7.4 Diffusion

Negligible diffusion for implanting silicon and magnesium atoms into GaN and annealed at 1,450°C [64] and for aluminum atoms implanted into 4H-SiC annealed at 1,700°C [65] has been observed by secondary ion mass spectrometry (SIMS). In contrast, the mechanism of boron diffusion in SiC has been considered to be very complicated. However, its understanding should become more important because the use of boron diffusion for fabricating 4H-SiC metal-insulator-semiconductor field-effect transistors was recently reported to reduce the interface state density near the conduction band edge of 4H-SiC [66].

7.4.1 Historic Background of Boron Diffusion in SiC

The first analysis of boron diffusion in SiC was based on a boron-vacancy model of 6H-SiC [67]. Detailed analysis of the boron-concentration profiles in nitrogen-doped 4H- and aluminum-doped 6H-SiC, however, indicated that I_{Si}, rather than V_{Si}, controls the diffusion of boron [68]. I_{Si}-mediated boron diffusion was then reconsidered in light of evidence of participation of I_C [69]. According to experiments on self-diffusion in isotopically enriched 4H-SiC, diffusivities of I_{Si} and I_C are of the same order of magnitude, and it was proposed that under specific experimental conditions, either defect is strongly related to the preferred lattice site of boron. Theoretical calculations of a 3C-SiC crystal structure [70–72] also showed that I_{Si} and

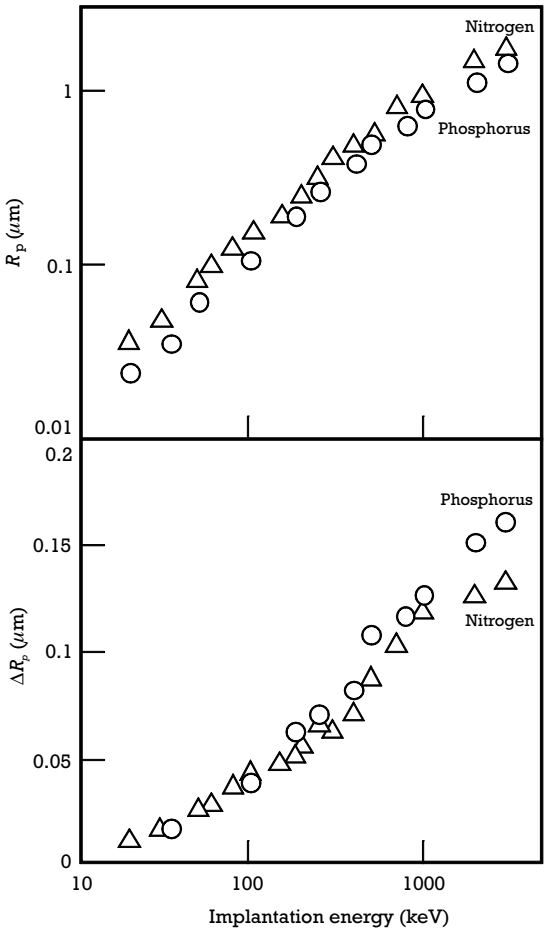

Figure 7.4 Projected range R_p and range straggling ΔR_p as a function of implantation energy in nitrogen and phosphorus ion implantation into SiC [49, 60–62].

I_C are far more mobile than V_{Si} and V_C. Under the assumption that I_{Si} and I_C have the same mobility in 4H-SiC, boron diffusion, via I_{Si} and I_C, can be simulated from a certain initial distribution of point defects.

Boron-related centers in SiC are known to have two key characteristics: a shallow acceptor with ionization energy of about 0.30 eV and a deep level with ionization energy of about 0.65 eV [73]. While the nature of the shallow acceptor defect is accepted as an off-center substitutional boron atom at a silicon site (B_{Si}) [74], that of the deep boron-related level is not clear. A B_{Si}-V_C pair [73] was refuted by *ab initio* calculations that suggest a B_{Si}-Si_C complex as a candidate [75]. In addition, candidates such as a substitutional boron atom at a carbon site (B_C) and a B_C-C_{Si} complex were also put

forward [76]. The boron-related deep center prevails in boron-doped 4H-SiC homoepitaxially grown under a silicon-rich condition [77], while similar experiments under a carbon-rich condition favor the shallow boron acceptor [69]. Since the site-competition effect suggests that boron atoms can occupy both silicon- and carbon-related sites, it is assumed that the deep boron-related level originates from B_C [69]. According to the theoretical results on 3C-SiC [70, 71], a mobile boron defect is a boron interstitial (I_B) rather than a boron-interstitial pair, which is considered to mediate boron diffusion in silicon [78, 79]. Although it is ideal to simulate diffusion of I_B to calculate boron-concentration profiles, the most relevant configuration of I_B in 4H-SiC is still not clear. To reproduce the experimentally obtained boron-diffusion profiles for designing 4H-SiC power devices, a boron-interstitial-pair diffusion model in a commercial process simulator [57], which is optimized mainly for use with silicon, is applied. The reported boron-concentration profiles in 4H-SiC [80, 81] are used in Sections 7.4.2 and 7.4.3 because the annealing conditions for high-temperature (500°C)-implanted (200 keV/4×10^{14} cm^{-2}) boron ions are systematically varied.

7.4.2 Dual-Sublattice Diffusion Modeling

It is assumed that I_{Si} and I_C diffuse on their own sublattices [82] in accordance with the theoretical calculation on boron diffusion in 3C-SiC [83]. The kick-out reactions forming I_B from a boron atom at the silicon site (B_{Si}) and at the carbon site (B_C) are then expressed as

$$B_{Si} + I_{Si} \leftrightarrow I_B(\text{type-I}) \tag{7.7}$$

$$B_C + I_C \leftrightarrow I_B(\text{type-II}) \tag{7.8}$$

where the expression for the charge state is omitted. In the case of 3C-SiC, I_B(type-I) and I_B(type-II) can be a carbon-coordinated tetrahedral site, a hexagonal site, or a split-interstitial at a silicon site or a carbon site [71]. The reactions given by (7.7) and (7.8) correspond to the following reactions in the boron-interstitial pair diffusion model [84]:

$$B_{Si}^{\,j} + I_{Si}^{\,m} \leftrightarrow (B_{Si}\, I_{Si})^u + (j+m-u)\ h^+ \tag{7.7a}$$

$$B_C^{\,k} + I_C^{\,n} \leftrightarrow (B_C\, I_C)^v + (k+n-v)\ h^+ \tag{7.8a}$$

with charge states $j, k, m, n, u, v \in \{0, \pm1, \pm2, \ldots\}$ and holes h^+. According to a previous calculation [71], I_{Si} in 3C-SiC can be charged from neutral to +4, and I_C from –2 to +2. If it is assumed that the variations in the charge

states of I_{Si} and I_C in 4H-SiC are the same as those in 3C-SiC, the ranges of m and n in (7.7a) and (7.8a) are limited to $m \in \{0, 1, 2, 3, \text{and } 4\}$ and $n \in \{0, \pm 1, \text{and } \pm 2\}$.

Boron diffusion in an epitaxially grown 4H-SiC structure with a buried boron-doped layer [85] is modeled as shown in Figure 7.5. In this case, the concentrations of point defects are considered to be in thermodynamic equilibrium. The Fermi model, in which all effects of point defects on dopant diffusion are built into pair diffusivities [86], is thus applied. In the present case, the pair diffusivities are $(B_{Si}I_{Si})^u$ and $(B_CI_C)^v$ in (7.7a) and (7.8a). In general, when the doping concentration exceeds the intrinsic carrier concentration n_i [87], where

$$n_i(T) = 1.70\times10^{16}\, T^{1.5} \exp(-2.08\times10^4/T)\ (\text{cm}^{-3}) \tag{7.9}$$

diffusion becomes concentration-dependent [86]. Diffusivity D of a pair (impurity A and interstitial I) is thus expressed as

$$D_{AI} = D_{AI}^{0} + D_{AI}^{+}(p/n_i)^{+1} + D_{AI}^{++}(p/n_i)^{+2} + D_{AI}^{-}(p/n_i)^{-1} + D_{AI}^{=}(p/n_i)^{-2} \tag{7.10}$$

where p is hole concentration, and superscripts "++" and "=" traditionally stand for +2 and –2. As described in the Section 7.4.1, boron atoms are incorporated into silicon sites as shallow acceptors (B_{Si}^{-}) when a SiC structure is grown under a carbon-rich condition. Equations (7.7a) and (7.10) thus become

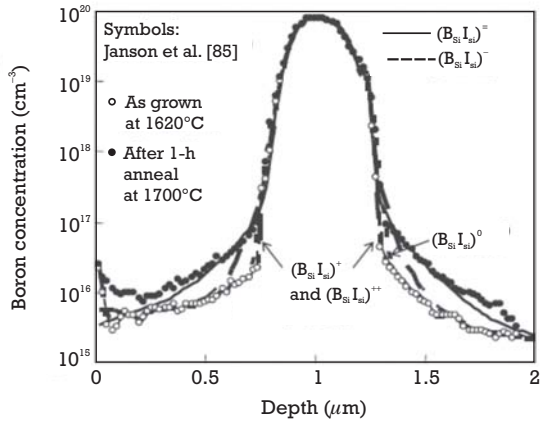

Figure 7.5 Boron-concentration profiles in an epitaxially grown 4H-SiC structure with a buried boron-doped layer before (open circles) and after one-hour annealing at 1,700°C [85]. The profile simulated using the diffusivity of a double-negatively charged $B_{Si}I_{Si}$ pair of 1×10^{-15} cm^2/s (solid curve) can precisely reproduce the experimental results (solid circles).

$$B_{Si}^{-}+I_{Si}^{m} \leftrightarrow (B_{Si}I_{Si})^{u}+(-1+m-u)\ h^{+} \tag{7.11}$$

$$\begin{aligned} D(B_{Si}I_{Si}) = {} & D(B_{Si}I_{Si})^{0}+D(B_{Si}I_{Si})^{+}(p/n_i)^{+1}+D(B_{Si}I_{Si})^{++}(p/n_i)^{+2} \\ & +D(B_{Si}I_{Si})^{-}(p/n_i)^{-}+D(B_{Si}I_{Si})^{=}(p/n_i)^{2} \end{aligned} \tag{7.12}$$

with $m \in \{0, 1, 2, 3, \text{and } 4\}$ and $u \in \{0, \pm1, \text{and } \pm2\}$.

It is assumed that a single term in the right-hand side of (7.12) dominates the diffusion of $(B_{Si}I_{Si})$ pairs. In Figure 7.5, the profile after one-hour annealing at 1,700°C was fitted by using one of the diffusivities of the following five $(B_{Si}I_{Si})$ pairs: neutral, single-, and double-positively charged, and single- and double-negatively charged. As shown in Figure 7.5, the profile simulated with the diffusivity of a double-negatively-charged $(B_{Si}I_{Si})$ pair of 1×10^{-15} cm^2/s can precisely reproduce the experimentally obtained concentration profiles, while the profiles simulated using the other four diffusivities cannot. $(B_{Si}I_{Si})^{=}$ is therefore chosen to simulate the diffusion of BSi^{-}.

The diffusion of B_C [71] is modeled next. Since B_C can be regarded as an acceptor, (7.8a) becomes

$$B_{C}^{-}+ I_{C}^{n} \leftrightarrow (B_{C}I_{C})^{v}+(-1+n-v)\ h^{+} \tag{7.13}$$

with n and $v \in \{0, \pm1, \text{and } \pm2\}$, and (7.10) becomes

$$\begin{aligned} D(B_{C}I_{C}) = {} & D(B_{C}I_{C})^{0}+D(B_{C}I_{C})^{+}(p/n_i)^{+1}+D(B_{C}I_{C})^{++}(p/n_i)^{+2} \\ & +D(B_{C}I_{C})^{-}(p/n_i)^{-1}+D(B_{C}I_{C})^{=}(p/n_i)^{-2} \end{aligned} \tag{7.14}$$

In the case of p-type 6H-SiC, the diffusivity of in-diffused boron is proportional to p when boron vapor pressure is low [68]. Under the assumption that similar dependence is observable in the case of 4H-SiC, Section 7.4.3 uses the diffusivity of a single-positively charged pair $(B_CI_C)^{+}$ to simulate the diffusion of B_C^{-}.

7.4.3 Semi-Atomistic Simulation

Diffusion of implanted boron ions is calculated from the initial point-defect distribution determined by Monte-Carlo simulation [82]. In the calculation, the continuity equation

$$\partial/\partial t\ (C_I+C_{(B_{Si}I)^{=}}+C_{(B_CI)^{+}}) = -\mathrm{div}(J_I+J_{(B_{Si}I)^{=}}+J_{(B_CI)^{+}})-K_r(C_IC_V-C_I^{*}C_V^{*}) \tag{7.15}$$

is solved with

$$J_{(B_{Si}I)^{=}} = -D_{(B_{Si}I)^{=}} \{-\text{grad}[C_{B_{Si}}{}^{-}(C_I/C_I^*)+C_{B_{Si}}{}^{-}(C_I/C_I^*)(qE/kT)]\} \tag{7.16}$$

and

$$J_{(B_CI)^{+}} = -D_{(B_CI)^{+}} \{-\text{grad}[C_{B_C}{}^{-}(C_I/C_I^*)+C_{B_C}{}^{-}(C_I/C_I^*)(qE/kT)]\} \tag{7.17}$$

where C_I and C_V are interstitial and vacancy concentrations, C_I^* and C_V^* are equilibrium interstitial and vacancy concentrations, J_I is the interstitial flux, K_r is the interstitial-vacancy bulk recombination coefficient, q is the electronic charge, E is the electric field, k is Boltzmann's constant, and T is the absolute temperature. As expressed by (7.16) and (7.17), both the fluxes of $(B_{Si}I)^{=}$ and $(B_CI)^{+}$ take the effect of electric field into account. The first step of the simulation is to obtain as-implanted boron profiles along with the initial distribution of point defects. Once I_{Si} and I_C are created, they are treated as the same I (with an unidentified origin). Similarly, the created V_{Si} and V_C are treated as the same V. Equations (7.12) and (7.14) are therefore simplified as

$$D_{(B_{Si}I)} = D_{(B_{Si}I)^{=}}(p/n_i)^{-2} \tag{7.18}$$

$$D_{(B_CI)} = D_{(B_CI)^{+}}(p/n_i)^{+1} \tag{7.19}$$

In the Monte-Carlo simulation, the surface of 4H-SiC was assumed to be misoriented by 8° from (0001) toward $[11\bar{2}0]$, and the boron-ion-beam divergence was set to 0.1°. The probabilities of the implanted boron ions occupying a silicon site (r_{Si}) or a carbon site (r_C) are specified as follows. For boron-ion implantation of 4×10^{14} cm^{-2} at 200 keV and 500°C [81, 82], as-implanted concentration profiles of B_{Si}^{-}, B_C^{-}, I, and V are calculated under the tentative assumption that $r_{Si} = r_C = 0.5$. The detailed procedure for determining other temperature-dependent parameters is described in [82].

As shown in Figure 7.6, owing to the introduction of the dual-sublattice modeling (described in Section 7.4.2), the simulated boron-concentration profiles well describe the tail regions of the measured profiles (symbols) with a background doping level (N_b) ranging from n- to p-type under conditions T = 1,900°C and t = 15 min [81]. The tail regions are represented mainly by B_{Si}^{-} ($N_b = 1 \times 10^{19}$ cm^{-3} [n-type]) and B_C^{-} ($N_b = 2 \times 10^{15}$ cm^{-3} [n-type] and 4×10^{19} cm^{-3} [p-type]). With respect to time-dependent diffusion, annealing-time (5 to 90 min) dependences of boron concentration

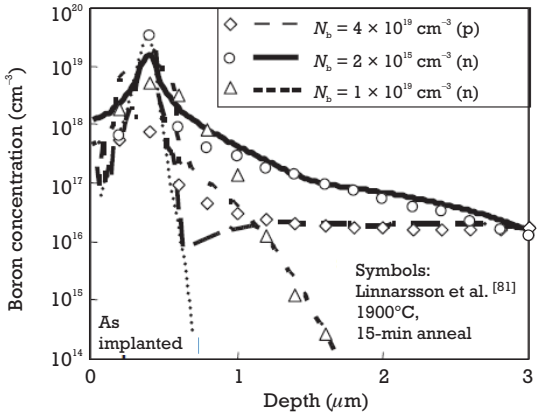

Figure 7.6 Measured (symbols [81]) and simulated boron-concentration profiles in 4H-SiC after 15-min annealing at 1900°C.

profiles for $N_b = 4 \times 10^{19}$ cm^{-3} (p-type) and $T = 1400$°C [81] are shown in Figure 7.7. The measured time-dependent boron-diffusion profiles (symbols) are precisely reproduced with parameters $D_{(B_{Si}I)}{}^{=} = 3 \times 10^{-18}$ cm^2/s, $D_{(B_CI)}{}^{+} = 6 \times 10^{-12}$ cm^2/s, and $K_r = 3 \times 10^{-16}$ cm^3/s.

The following remaining issue should also be noted: For applying the developed semi-atomistic simulation to fit other experimentally obtained boron-concentration profiles, r_{Si}/r_C must be optimized. Since this optimization is strongly related to experimental conditions [69], r_{Si}/r_C needs to be optimized for each experimental condition.

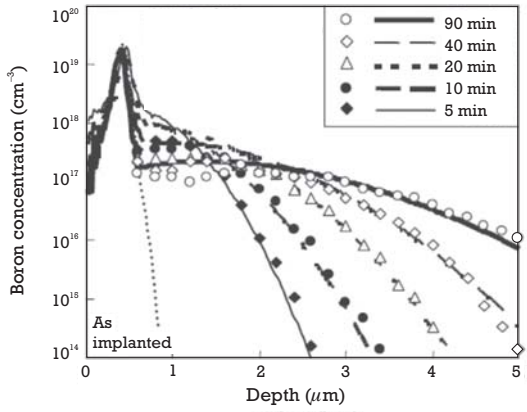

Figure 7.7 Measured (symbols [81]) and simulated boron-concentration profiles in 4×10^{19}-cm^{-3}-doped p-type 4H-SiC after annealing at 1,400°C.

7.5 Oxidation

In the case of silicon, thermal oxidation represents the most useful method for oxide growth because of a high-quality oxide/semiconductor interface and convenience in terms of device fabrication. However, thermal oxidation of compound semiconductors is much more complex phenomenon than that of silicon.

7.5.1 Thermal Oxidation of GaN

He-Cd laser illumination has been used to grow 80-nm-thick α-Ga_2O_3 by oxidizing GaN in an H_3PO_4 solution (with pH of 3.5) [88]. This technique has also been applied to fabricating AlGaN/GaN metal-insulator-semiconductor (MIS) high electron mobility transistors [89]. However, among the five phases of Ga_2O_3, α is a metastable phase; the most stable phase of Ga_2O_3 is β.

Although β-Ga_2O_3 was obtained by oxidizing GaN at 850 °C for 12 h in an oxygen ambient [90], a very small conduction-band discontinuity, ΔE_C, of 0.1 eV (Figure 7.8 [91]) limits its use as a gate dielectric for GaN MIS field-effect transistors (MISFET) (compare ΔE_C = 2.3 eV in the case of a deposited SiN_x layer on GaN and ΔE_C = 2.1 eV in the case of a deposited Al_2O_3 layer on GaN [92]).

7.5.2 Thermal Oxidation of 4H-SiC

Thermal oxidation of SiC is expressed as

$$2SiC+3O_2 \rightarrow 2SiO_2+2CO \tag{7.20}$$

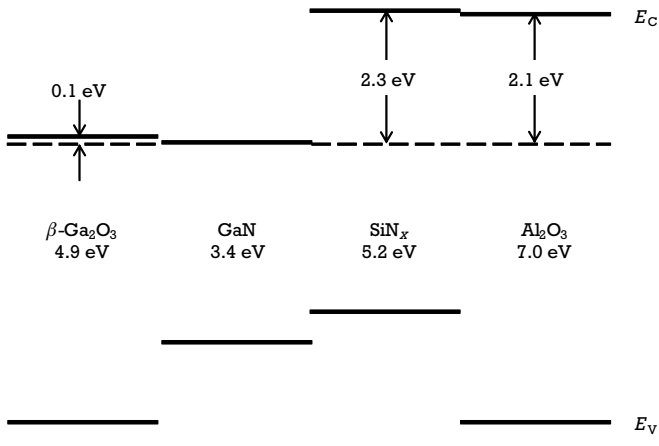

Figure 7.8 Reported energy band alignment at room temperature [91, 92].

where CO molecules ideally diffuse out of the growing oxide. However, some carbon atoms possibly remain near the oxide/SiC interface. Although the measured dependences of oxide thickness on oxidation time have been explained by the so-called Deal–Grove model [93, 94], deviation from this model has been pointed out [95]. Microscopic understanding of thermal oxidation is thus yet to be established. With respect to ΔE_C of the thermal oxide/4H-SiC, ΔE_C on (0001) (i.e., 2.7–2.8 eV) was reported to be larger than ΔE_C on $(000\overline{1})$ (2.3–2.5 eV) [96]. This difference in ΔE_C possibly comes from a dipole at the interfaces of the oxide and 4H-SiC polar (0001) faces.

The use of an oxide deposited on 4H-SiC and nitrided in NO or N_2O was found to be more reliable compared to oxides formed by N_2O oxidation and O_2 oxidation [97]. A pileup of nitrogen at the oxide/SiC interface reportedly contributed to the improvement of the interface quality [98].

7.6 Metallization

Since Schottky contacts are described in Chapter 8, n- and p-ohmic contacts are introduced as follows.

7.6.1 Ohmic Contacts to GaN

Titanium/aluminum and titanium/aluminum-based multilevel structures (e.g., gold/nickel/aluminum/titanium) are commonly used as ohmic contacts to n-GaN [99]. A low specific contact resistance ρ_c of less than 10^{-5} Ωcm^2 was achieved using titanium/aluminum annealed at 900°C for 20 s [100]. With respect to contacts with n^+GaN (whose donor density is in the order of 10^{19} cm^{-3}), tungsten and tungsten silicide (WSi_x) also led to low ρ_c (8×10^{-5} Ωcm^2 [101]).

As for ohmic contacts to p-GaN, palladium and palladium-based contacts (including gold/palladium, gold/platinum/palladium, and gold/palladium/magnesium/palladium) show ohmic characteristics even before annealing [102]. This finding was explained by a "disorder-induced gap state (DIGS) model" [103] in which Fermi-level pinning occurs due to stress in the epitaxial Pd (111)/p-GaN (0001) interface [104]. A very low ρ_c of 1×10^{-6} Ωcm^2 was reported in the case of gold/titanium/gold/silver/palladium alloyed at 800°C for 1 min in flowing nitrogen ambient [105].

7.6.2 Ohmic Contacts to 4H-SiC

A 50–100-nm-thick nickel layer becomes a good n-ohmic contact with 4H-SiC ($\rho_c = 1 \times 10^{-6}$ Ωcm^2 at a donor density of 2×10^{19} cm^{-3}) when sintered at around 1,000°C [106, 107]. The carbon atoms that accumulated near the

metal/semiconductor interface were suggested to lower ρ_c [108]; however, the detailed mechanism is not fully understood [107].

As for p-ohmic contacts with 4H-SiC, aluminum-based metal (e.g., titanium/aluminum and titanium/nickel/aluminum) are known [109, 110]. To obtain ρ_c of less than 1×10^{-5} Ωcm^2, acceptor concentration exceeding 3×10^{19} cm^{-3} was needed when sintering was performed at 1,000°C for 2 minutes [111]. To avoid using low-melting-point (about 630°C) aluminum, palladium-based [112], nickel-based [113], and titanium-based p-ohmic contacts [114] have also been investigated.

7.7 Passivation

Since the surface of a semiconductor is sensitive to a high-electric field, the free bonds of the surface atoms must be terminated. As a passivation layer, SiO_2 is often used for both GaN and 4H-SiC power devices.

Other than SiO_2, high-dielectric-constant (high-k) film has been applied for GaN diodes. A high-k film generates a greater expanded depletion region than that generated using a SiO_2 film with the same thickness, so higher breakdown voltage devices are expected. A mixed oxide of SiO_2 and CeO_2 (k = 12.3) was formed on mesa-type GaN p^+n diodes using MOCVD [115–117]; the resultant breakdown voltage exceeded 2 kV, while that of diodes passivated with SiO_2 (k = 3.9) was 1 kV [118].

With respect to the application of high-k film to 4H-SiC power devices, a field plate (see Chapter 11) using HfO_2 was simulated [119]. The simulation results showed that a high-k field plate can significantly relieve electric-field enhancement and increase breakdown voltage.

7.8 Summary

Following Chapter 6 on epitaxial growth, this chapter describes the basic aspects of fabrication processes for GaN and 4H-SiC power devices. Readers should also refer to the latest papers on oxidation of 4H-SiC as related research is still being actively conducted.

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CHAPTER

8

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Metal-Semiconductor Contacts and Unipolar Power Diodes

8.1 Introduction

As described in Chapter 1, a power diode, which exhibits forward voltage drop V_F at forward current I_F (Figure 1.8), is one of the building blocks of power-electronic circuits. In the case of a bipolar diode, qV_F takes a value approximately equivalent to the bandgap energy E_g of the semiconductor used, where q is elementary charge (1.6×10^{-19} C). For example, the measured forward-current/voltage characteristics of a GaN p^+n diode (Figure 8.1[a]) [1] (which is shown in Figure 3.6) are plotted on a linear scale in Figure 8.1(b). At I_F of 5.2 mA (i.e., 180 A/cm^2), V_F becomes E_g/q of GaN (i.e., 3.44V [2]). To further decrease V_F, a unipolar diode must therefore be used. Another advantage of a unipolar diode is absence of minority-carrier injection, leading to a very fast turnoff and low switching energy.

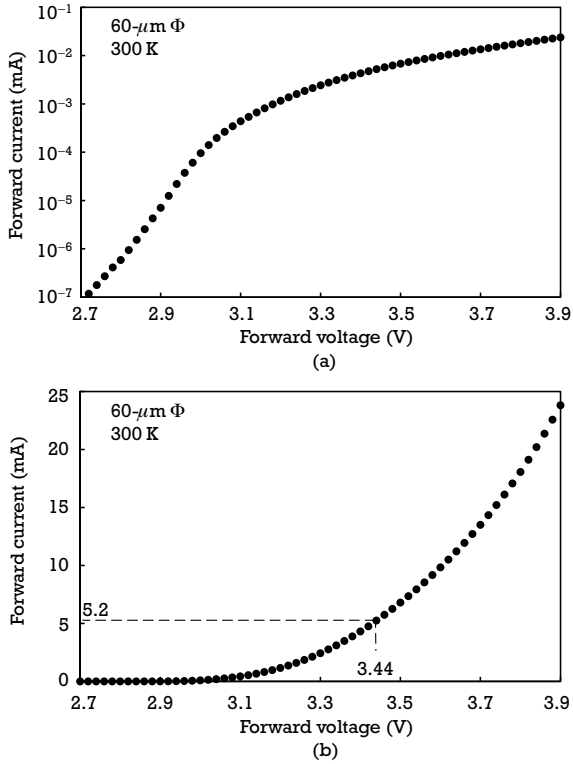

Figure 8.1 Room-temperature forward-current/voltage characteristics of a GaN p^+n diode plotted on (a) semi-log [1] and (b) linear scales.

A unipolar diode utilizes a metal-semiconductor contact called a Schottky junction [3]. An energy-band diagram of a metal and an n-type semiconductor that are not in contact is shown in Figure 8.2(a). The vacuum or free-electron energy is taken as a reference level that represents the energy that an electron would have if it were free of influence of the metal or the semiconductor. The difference between the vacuum level and Fermi level (see Section 2.3) is called the work function, which is usually denoted as $q\Phi$ in eV (or Φ in volts). In the case of semiconductors, the work function becomes a function of dopant concentration. Since electron affinity $q\mathrm{X}$ (i.e., the difference between the vacuum level and the conduction-band minimum, E_C) is constant, the work functions of the metal and the semiconductor are respectively expressed as $q\Phi_m$ and $q(\mathrm{X} + \Phi_n)$ in Figure 8.2(a), where $q\Phi_n$ is the difference between E_C and the Fermi level E_F of the semiconductor. Hereafter, the case that $\Phi_m > \mathrm{X} + \Phi_n$—namely, the electrons in the semiconductor have a higher total energy (on average) than the electrons in the metal—is considered.

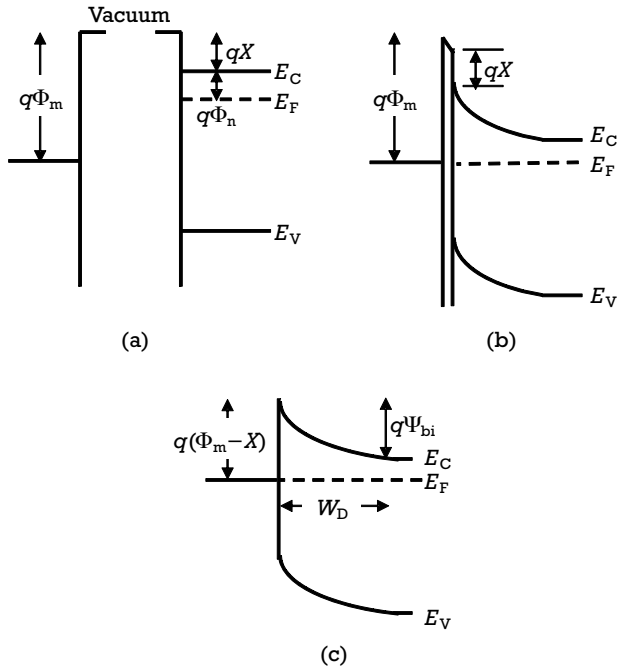

Figure 8.2 Energy-band diagrams of a metal and an n-type semiconductor (a) in separation and connected with (b) finite and (c) no gaps.

When the metal and the semiconductor are almost in contact and separated with a finite gap (Figure 8.2[b]), the Fermi level of the metal, which is equal to $q\Phi_m$, coincides with the E_F of the semiconductor in equilibrium. Note that in Figure 8.2(b) the vacuum level is continuous and the electron affinity is constant. In the case that the gap between the metal and the semiconductor becomes zero (Figure 8.2[c]), an abrupt discontinuity of E_C exists at the metal-semiconductor interface. The magnitude of this discontinuity is called the Schottky-barrier height ($q\Phi_B$), which is expressed as

$$q\Phi_B = q(\Phi_m - X) = q(\Psi_{bi} + \Phi_n) \tag{8.1}$$

Since $q\Phi_B$ is smaller than E_g (= $E_C - E_V$) of the semiconductor, V_F of a unipolar diode is less than V_F of a bipolar diode as long as the voltage-drop across the drift layer is negligible.

8.2 Schottky-Barrier Lowering

Schottky-barrier lowering is the lowering of $q\Phi_B$ induced by an image force in the presence of electric field. In detail, when an electron is at

a distance x from a metal surface, a positive charge is induced on the metal surface. The attractive force between the electron and the positive charge is equivalent to the attractive force F between the electron and an equal positive charge located at $-x$ (i.e., the image charge) given as

$$F = -q^2/[4\pi\varepsilon_r\varepsilon_o(2x)^2] = -q^2/(16\pi\varepsilon_r\varepsilon_o x^2) \tag{8.2}$$

The work done on the electron in the course of its transfer from the point x to infinity is given as

$$W(x) = \int_x^\infty F dx = -q^2 / \left(16\pi\varepsilon_r\varepsilon_o x^2\right) \tag{8.3}$$

Equation (8.3) corresponds to the potential energy $E_p(x)$ of an electron placed at distance x from the metal surface. Under electric field E, $E_p(x)$ is lowered from $-q|E|x$ as follows:

$$E_p(x) = -q|E|x - q^2/(16\pi\varepsilon_r\varepsilon_o x) \tag{8.4}$$

$E_p(x)$ reaches a maximum at x_m, which is given as

$$x_m = [q/(16\pi\varepsilon_r\varepsilon_o|E|)]^{0.5} \tag{8.5}$$

under the condition $dE_p/dx = 0$. $q\Phi_B$ is thus reduced from the value at $x = 0$ [(8.1)] by $\Delta q\Phi_B$, which is given by

$$\Delta q\Phi_B = (qE_{max}/4\pi\varepsilon_r\varepsilon_o)^{0.5} \tag{8.6}$$

where E_{max} is maximum field strength (see Section 3.5).

8.3 Forward-Biased Schottky Junction

Two distinctly different mechanisms exist in forward current across a Schottky junction: thermionic emission of carriers across the Schottky barrier [4] and diffusion of carriers from the semiconductor into the metal [3] (Section 8.4). The thermionic emission theory postulates that only energetic electrons, which have an energy equal to or larger than the conduction band energy at the metal-semiconductor interface, contribute to forward current J_{TE} (8.7). The diffusion theory, on the other hand, assumes that the driving force for forward current J_D (8.8) is distributed over the length of the depletion layer.

$$J_{TE} = qN_C(kT/2\pi m_n)^{0.5} \exp(-q\Phi_B/kT)\ [\exp(qV_F/kT)-1] \tag{8.7}$$

and

$$J_D = (q^2 D_n N_C/kT)\{[2q(\Phi_B-\Phi_n-V_F)N_D]/\varepsilon_r\varepsilon_o\}^{0.5} \times \exp(-q\Phi_B/kT)\ [\exp(qV_F/kT)-1] \tag{8.8}$$

where N_C is the effective density of states in conduction bands (2.6b), m_n is the effective mass of electrons, and D_n is the diffusivity of electrons (Section 3.2).

In the case of a silicon Schottky junction, forward current is limited by J_{TE}; however, this is not the case with GaN and 4H-SiC Schottky junctions due to the following reason. The charge and field distributions and band diagrams for a metal-semiconductor junction are similar to those of a p^+n junction shown in Figure 3.4. When forward voltage V_F is applied to the metal and the semiconductor is grounded, E_{max} is given by (3.28) and (3.31) as

$$E_{max} = [2qN_D(\Psi_{bi}-V_F)/\varepsilon_r\varepsilon_o]^{0.5} \tag{8.9}$$

For example, breakdown voltage BV is about 0.5 kV when N_D is 5×10^{14} cm^{-3} in the case of a silicon Schottky junction, and N_D is 1×10^{17} cm^{-3} in the cases of GaN and 4H-SiC Schottky junctions [5]. When $\Psi_{bi} - V_F$ is 0.1V, E_{max} is 4 kV/cm in the case of the silicon Schottky junction and 60 kV/cm in the cases of the GaN and 4H-SiC Schottky junctions. Although the drift velocity of electrons (v_n) in the case of the silicon Schottky junction is almost proportional to $|E|$, v_n almost saturates in the cases of the GaN and 4H-SiC Schottky junctions (Figure 8.3) [6–8].

Einstein relation (see [3.6a]) changes a little under high E_{max} as follows:

$$D_n = (akT/q)\ \mu_n(E) \tag{8.10}$$

where $a = 1.5$ in the case of n-type GaN under E_{max} of 60 kV/cm [9]. Equation (8.8) then becomes

$$J_D = aq\mu_n(E_{max})N_C E_{max} \exp(-q\Phi_B/kT)\ [\exp(qV_F/kT)-1] \tag{8.11}$$

When E_{max} is 60 kV/cm, μ_n is 345 and 164 cm^2/Vs (Figure 8.3), respectively, for n-type GaN and 4H-SiC. These high-field μ_n values are much lower than low-field $\mu_n{}^{GaN}$ of 1,000 cm^2/Vs and $\mu_n{}^{4H\text{-}SiC}$ of 1,140 cm^2/Vs [10]. This condition means that collisions of electrons with the lattice (i.e.,

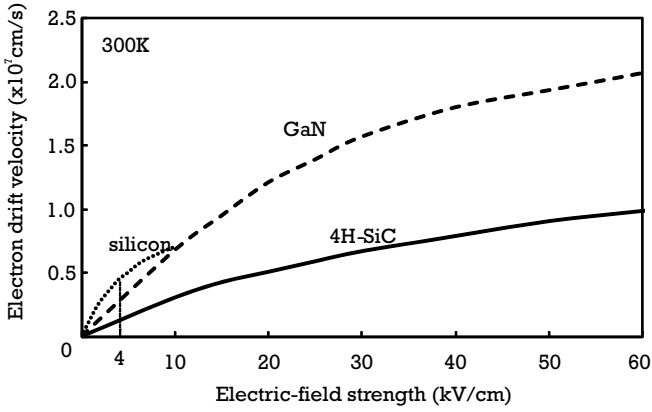

Figure 8.3 Electric-field strength dependences of drift velocities of electrons in n-type GaN, 4H-SiC, and silicon [6–8].

diffusion) significantly contribute to electrons in n-type GaN or 4H-SiC reaching the Schottky junction (Figure 8.4) [11–13]. However, in the literature on GaN and/or SiC power devices, thermionic emission is described as the controlling forward-current-conduction mechanism of a Schottky junction [14–17]. Therefore, forward-current/voltage characteristics based on diffusion [3] and thermionic emission diffusion (TED) [18] are introduced in Sections 8.4 and 8.5.

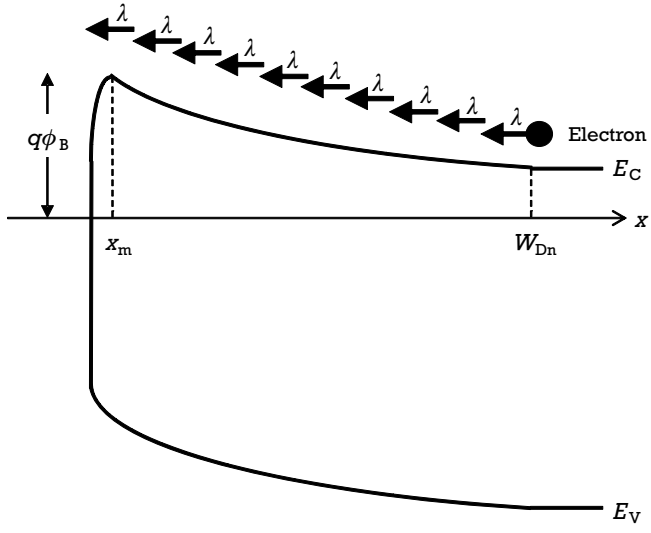

Figure 8.4 Schematic band diagram of a forward-biased GaN or 4H-SiC Schottky junction. λ denotes electron mean free path.

8.4 Forward-Current/Voltage Characteristics Based on Diffusion Theory

According to the diffusion theory proposed by Schottky [3], W_{Dn} is assumed to be sufficiently larger than λ (which is the case with GaN and 4H-SiC Schottky junctions) so using diffusivity and mobility of electrons for analyzing current/voltage characteristics is practical. According to that diffusion theory, the dependence of forward-current density (J_{D}) on forward voltage (V_{F}) in a Schottky junction is obtained by integrating the equation for electron diffusion and drift (see [3.10a]), namely,

$$J_{\mathrm{D}} = qn\mu_{\mathrm{n}}E + qD_{\mathrm{n}}(\partial n/\partial x) \tag{8.12}$$

across the depletion region near the Schottky junction. If the potential is denoted as Φ,

$$E = -\partial\Phi/\partial x \tag{8.13}$$

Using the Einstein relation (see [3.6a]), for an n-type semiconductor, namely,

$$D_{\mathrm{n}} = (kT/q)\,\mu_{\mathrm{n}} \tag{8.14}$$

(8.12) can be written as

$$J_{\mathrm{D}} = qD_{\mathrm{n}}[-(qn/kT)(\partial\Phi/\partial x) + \partial n/\partial x] \tag{8.15}$$

By multiplying both sides of (8.15) by an integrating factor, $\exp(-q\Phi/kT)$, before integration and assuming that J_{D} is not a function of x, (8.15) becomes

$$J_D\int_0^{W_{Dn}} \exp\left(-q\Phi / kT\right)dx = qD_n\left[n\exp\left(-q\Phi / kT\right)\right]_0^{W_{Dn}} \tag{8.16}$$

If $\Phi(0)$ is defined as zero, $\Phi(W_{\mathrm{Dn}})$ becomes $\Phi_{\mathrm{B}} - \Phi_{\mathrm{n}} - V_{\mathrm{F}}$. Equation (2.12a) is used to express $n(W_{\mathrm{Dn}})$ and $n(0)$ as

$$n(W_{\mathrm{Dn}}) = N_{\mathrm{C}} \exp(-q\Phi_{\mathrm{n}}/kT) \tag{8.17a}$$

and

$$n(0) = N_{\mathrm{C}} \exp(-q\Phi_{\mathrm{B}}/kT) \tag{8.17b}$$

Substituting these boundary values into (8.16) gives

$$J_D = qD_n N_C \exp(-q\Phi_B / kT)\left[\exp(qV_F / kT) - 1\right] / \int_0^{W_{Dn}} \exp(-q\Phi / kT)\,dx \tag{8.18}$$

By integrating (3.27b), it is possible to approximate $\Phi(x)$ as

$$\Phi(x) = (qN_D/\varepsilon_r\varepsilon_o)x(W_{Dn} - x/2) \text{ for } 0 < x < W_{Dn} \tag{8.19}$$

When (8.19) is inserted into (8.18), and integrating the substituted equation, J_D is obtained as a function of V_F as

$$J_D = J_{DS}\,[\exp(qV_F/kT) - 1] \tag{8.20a}$$

and

$$J_{DS} = (q^2 D_n N_C/kT)\{[2q(\Phi_B - \Phi_n - V_F)N_D]/\varepsilon_r\varepsilon_o\}^{0.5} \exp(-q\Phi_B/kT) \tag{8.20b}$$

In (8.20b), the square-root dependence of J_{DS} on V_F is weak; therefore, it is possible to approximate (8.20a) as

$$J_D = J_{DS}'\,[\exp(qV_F/nkT) - 1] \tag{8.21}$$

where J_{DS}' is independent of V_F and n is an ideality factor(Section 3.6.1.1).

8.5 Forward-Current/Voltage Characteristics Based on TED Theory

In Section 8.4, the Schottky junction is assumed to be almost at thermal equilibrium even though currents are flowing. In this section, the influence of thermionic emission on current/voltage characteristics is also considered through the boundary condition of thermionic-recombination velocity v_R at x_m. Here, the case that $q\Phi_B$ is large enough that the charge concentration between the metal surface and $x = W_{Dn}$ (Figure 8.4) is that of ionized donors is considered. Under the assumption that the portion of the barrier between $x = 0$ and x_m acts as a sink for electrons, forward-current density based on TED is expressed as

$$J_{TED} = \{A^* T^2/[1 + (v_R/v_D)]\}\exp(-q\Phi_B/kT)[\exp(qV/kT) - 1] \tag{8.22a}$$

$$v_R = (A^*T^2/2q)(2\pi m_n kT/h^2)^{-1.5} \tag{8.22b}$$

$$v_D = \left(\mu_n kT/q\right)\exp\left(q\Phi_B/kT\right)/\int_0^{W_{Dn}} \exp\left[E_C(x)/kT\right]dx \tag{8.22c}$$

$$E_C(x) = q\Phi_B - (q^2 N_D/2\varepsilon_r\varepsilon_o)(2W_{Dn}x - x^2) \tag{8.22d}$$

and

$$A^* = 4\pi m_n k^2 q/h^3, \tag{8.22e}$$

where $E_C(x)$ is the conduction-band-edge energy measured from the Fermi level in the metal, v_D is the effective diffusion velocity associated with the transport of electrons from W_{Dn} to x_m, h is the Planck constant (6.6×10^{-34} Js), and A^* is the effective Richardson constant. For free electrons, A^* is equal to the Richardson constant A of 120 $Acm^{-2}K^{-2}$. Since GaN has isotropic effective mass ($0.20 \times 9.1 \times 10^{-31}$ kg) in the lowest minimum of the conduction band, A^*/A is simply equal to 0.20. In the case of 4H-SiC, on the other hand, A^*/A becomes 1.2 because the number of conduction band minima is 6 [19].

In (8.22a), v_R/v_D determines the relative current-limiting factor of TE versus diffusion. In the case of a GaN Schottky junction, J_{TED} is limited by the diffusion process at elevated temperatures due to reduced μ_n [12] (see Section 8.7.1). In the case of a shielded 4H-SiC Schottky junction fabricated using ion implantation (see Section 8.10.2), the influence of the diffusion process on current/voltage characteristics is large even at room temperature [13]. Note that numerical analysis is convenient for simultaneously considering TE and diffusion [11].

8.6 Reverse-Current/Voltage Characteristics Based on TFE Theory

When negative bias V_R is applied to a metal/n-type semiconductor Schottky junction, a voltage is applied across the depletion region formed in the n-type semiconductor. In the cases of GaN and 4H-SiC Schottky junctions, the resulting tunneling current due to large E_{max}, which is an order of magnitude larger than E_{max} in the case of a silicon Schottky junction, cannot be ignored. Electron tunneling near the Fermi level is called field emission (FE), while tunneling of thermally excited electrons, which face a thinner barrier than FE, is called thermionic-field emissions (TFE) (Figure 8.5). FE dominates when thermal energy kT is much lower than E_{00}, which is defined as

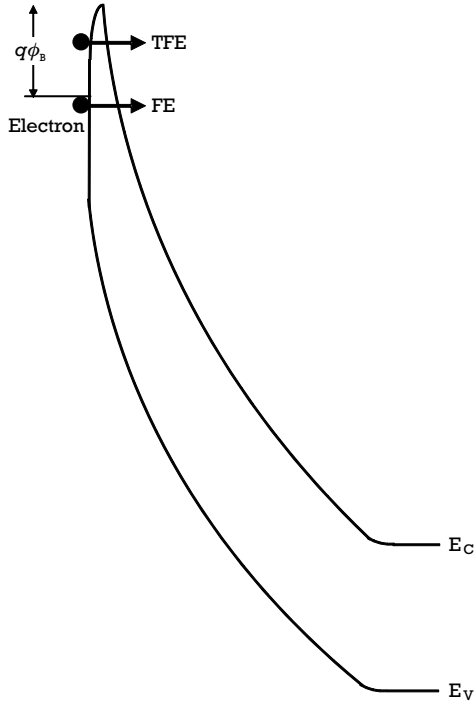

Figure 8.5 Schematic energy-band diagram showing electron tunneling (i.e., FE and TFE) through a reverse-biased Schottky junction.

$$E_{00} = (qh/4\pi)\ (N_D/m_n\varepsilon_r\varepsilon_o)^{0.5} \tag{8.23}$$

As shown in Figure 8.6, kT is lower than E_{00} when $N_D > 10^{15}$ cm^{-3} and $T < 15$K. At room temperature, on the other hand, $kT >> E_{00}$ when $N_D < 10^{16}$ cm^{-3}, indicating the dominance of TFE over FE.

Current/voltage characteristics calculated under the assumption of TFE was reported to agree with the reverse characteristics of 100-μm-diameter nickel/GaN Schottky-barrier diodes (SBDs) [20]; however, it did not agree with the reverse characteristics of large (9-mm^2) nickel/GaN SBDs [21]. Moreover, in the case of 4H-SiC SBDs, threading-dislocation density was reported to influence the measured reverse characteristic; for example, maximum reverse current density (2×10^{-1} mA/cm^2 at 0.6 kV) of 53 molybdenum/4H-SiC SBDs was four-orders-of-magnitude larger than minimum reverse current density (2×10^{-5} mA/cm^2 at 0.6 kV) [22] (Figure 8.7). These findings suggest that describing an equation for J_{TED} under the reverse-biased condition with (8.22a) is not much use. Instead, structures that minimize reverse current (namely, insertion of a wider-bandgap

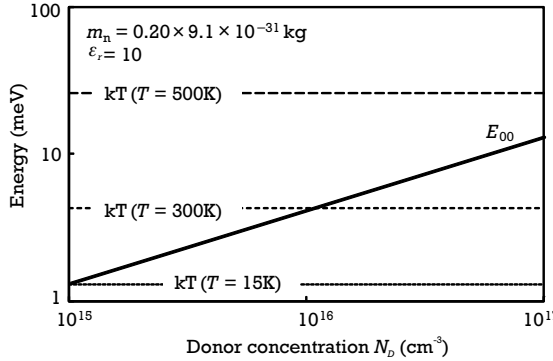

Figure 8.6 Calculated E_{00} (8.23) versus thermal energy as a function of donor concentration.

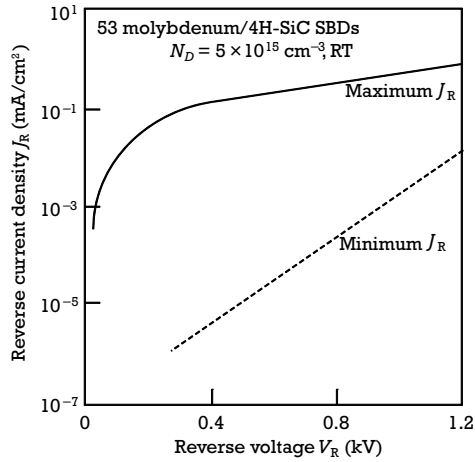

Figure 8.7 Maximum and minimum reverse current-density/voltage characteristics of molybdenum/4H-SiC SBDs measured at room temperature [22].

or a thin p^+-type semiconductor layer, and/or lower E [Figure 8.8]) are introduced after planar SBDs are introduced.

8.7 Pure SBDs

8.7.1 Pure GaN SBDs

In 2001, availability of freestanding GaN substrates made it possible to fabricate the 450-V and 700-V vertical GaN SBDs [23, 24], shown in Figure 8.9(a) (hereinafter called pure GaN SBDs), for the first time. The backside ohmic contacts were titanium/aluminum [23] or titanium/aluminum/

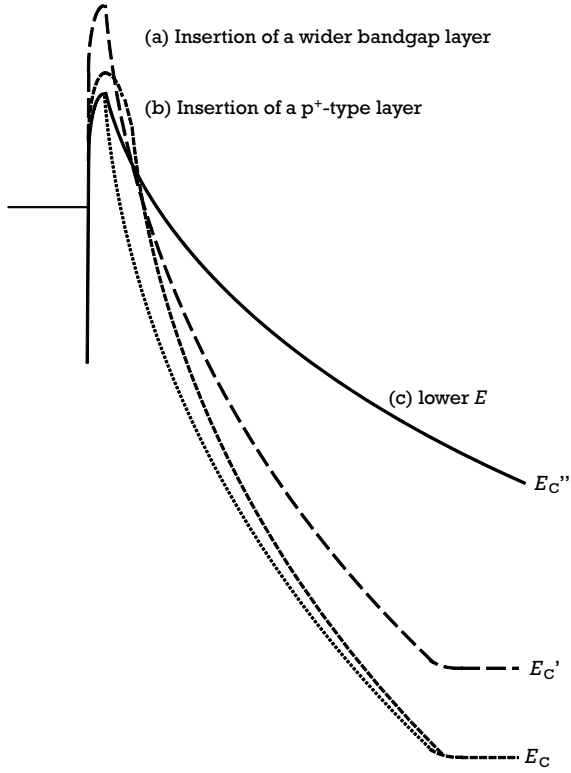

Figure 8.8 Schematic conduction-band diagrams for suppressing electron tunneling through a reverse-biased Schottky junction. In (a) and (b), a wider-bandgap semiconductor layer or a thin p^+-type layer is inserted at the Schottky junction, while in (c) the electric field (solid line) is lower than those shown in Figure 8.5.

platinum/gold [24], while the Schottky contact was platinum/gold [23] or platinum/titanium/gold [24]. However, N_D was relatively large—namely, $> 5 \times 10^{16}$ cm^{-3} [23], and in the order of 10^{17} cm^{-3} [24]. In 2006, N_D of 7×10^{15} cm^{-3} was used for fabricating 600-V pure GaN SBDs on GaN substrates [25, 26]. The first pure GaN SBDs with a lightly doped epitaxial layer ($N_D = 1 \times 10^{14}$ cm^{-3}) grown on n^+ GaN substrates were fabricated with edge termination (see Chapter 11) by argon-ion implantation [27, 28]. The reported *BV* was 1.3 kV.

Pure SBDs using high-quality GaN (μ_n = 930 cm^2/Vs) were first fabricated in 2010 by using nickel/gold Schottky contact metal and field-plate edge termination [29] (see Chapter 11). *BV* was 1.1 kV, and forward current I_F exceeded 10A with relatively low V_F of 1.46V at J_F = 500 A/cm^2. In 2015, 9-mm^2 pure GaN SBDs with both high I_F (50A) and high *BV* (0.79 kV) were fabricated by using nickel Schottky contact metal and mesa field-plate

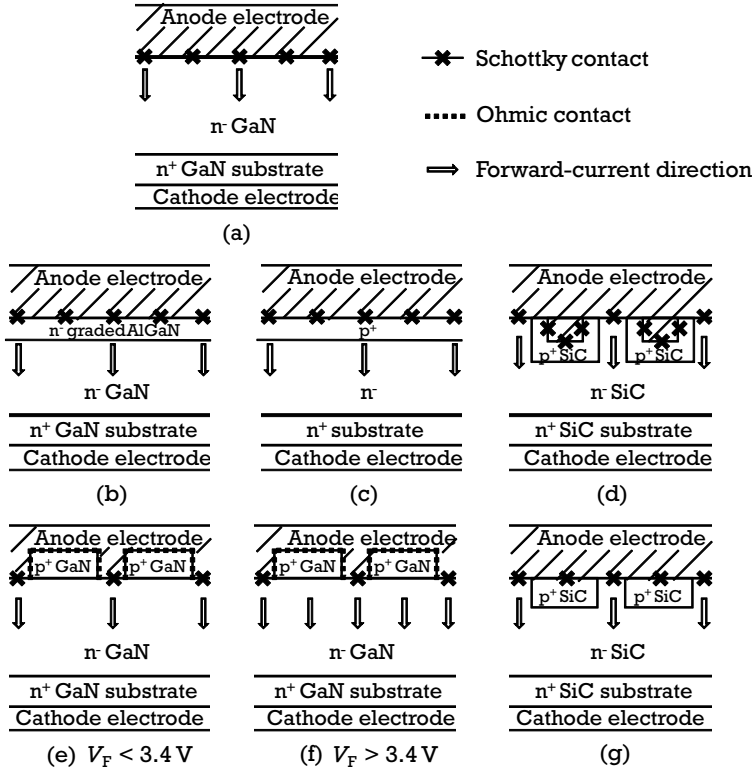

Figure 8.9 Cross-sectional schematic illustrations of active regions of SBDs: (a) pure SBD, (b) SBD with a wider-bandgap layer, (c) SBD with a thin p^+-type layer, (d) trench SBD with a thin p^+-type region, (e, f) GaN merged p-n Schottky (MPS) diode, and (g) 4H-SiC junction-barrier Schottky (JBS) diode.

edge termination [21] (see Chapter 11). As shown in Figure 8.10(a), V_F was 1.30V for a typical limit on power dissipation of a semiconductor package (P_P = 300 W/cm^2 [30]).

With increasing temperature, μ_n decreases as a result of phonon scattering. Dependence of $q\Phi_B$ on temperature (348–573K) was analyzed by fitting measured I_F/V_F characteristics of a nickel/n-GaN pure SBD on the basis of the TED model [12].

8.7.2 Pure 4H-SiC SBDs

The first-reported high-voltage pure SiC SBDs with low V_F (1.1 V at J_F = 100 A/cm^2) were 6H polytype [31]. The Schottky metal was platinum, and *BV* was 400V. *BV* was later improved with edge termination using argon-ion implantation [32] (see Chapter 11). With respect to pure 4H-SiC SBDs, *BV*

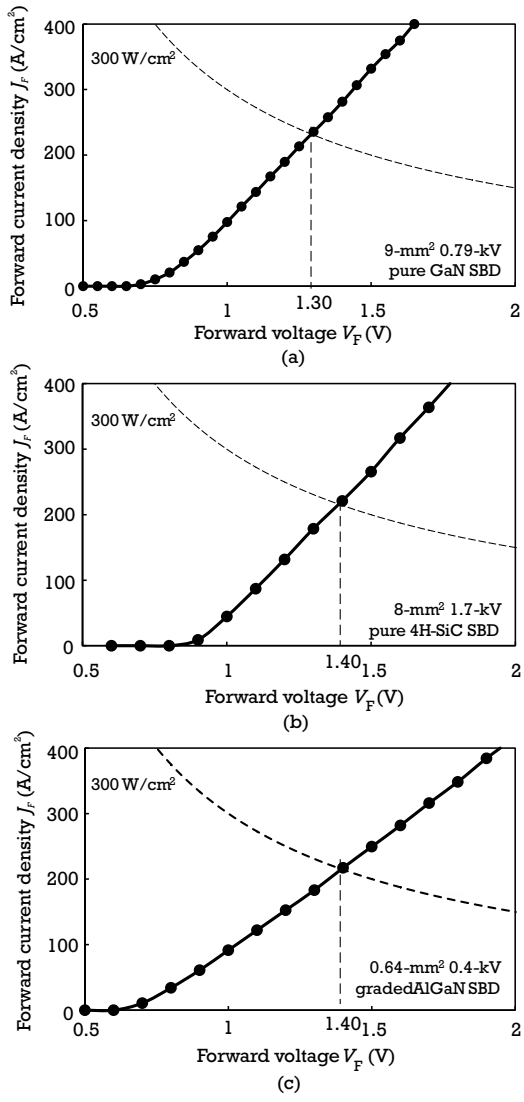

Figure 8.10 Forward-current-density/voltage characteristics of (a) 9-mm^2 0.79-kV pure GaN SBD [21], (b) 8-mm^2 1.7-kV pure 4H-SiC SBD [33], and (c) graded AlGaN SBD [34] measured at room temperature.

ranging from 1.5 to 2.5 kV with V_F of 2.4V at J_F = 100 A/cm^2 [35], *BV* of 4 kV with V_F of 6V at J_F = 100 A/cm^2 [36], and *BV* of 4.9 kV with V_F of 2.4V at J_F = 25 A/cm^2 [37] were achieved by using nickel Schottky contact metal. Pure molybdenum/4H-SiC SBDs with BV of 4.15 kV with V_F of 1.89V at J_F = 100 A/cm^2 were also fabricated [38].

As an example of pure 4H-SiC SBDs with large I_F, J_F-V_F characteristics of a reported 8-mm^2 1.7-kV SBD [32] are shown in Figure 8.10(b). According to Figure 8.10(b), V_F is 1.40V for P_P of 300 W/cm^2.

8.8 Graded AlGaN SBDs

With respect to vertical SBDs with a wider-bandgap layer (Figure 8.9[b]), GaN SBDs with a graded AlGaN layer have been fabricated by using palladium [39] and nickel/gold [33] Schottky contact metals. Due to the existence of oxygen shallow donors (e.g., energy depth of 0.03 eV [40, 41] for $Al_{0.26}Ga_{0.74}N$) that reduce $q\Phi_B$ (thin-surface-barrier [TSB] model) [42], however, analyzing their J_R/V_R characteristics tends to be complicated [39]. As shown in Figure 8.10(c), V_F of a reported 0.64-mm^2 0.4-kV graded AlGaN SBD [32] is 1.40V (for P_P of 300 W/cm^2), which is 0.1V larger than V_F of the pure GaN SBD shown in Figure 8.10(a).

8.9 4H-SiC SBDs with a Thin p$^+$-Type Layer

With respect to a SBD with a p$^+$-type layer (thickness: a) (Figure 8.9[c]), an idealized profile of net donor concentration (N_D–N_A) is shown in Figure 8.11(a). Distribution of electric field E shown in Figure 8.11(b) is expressed as

$$\begin{aligned} E &= E_{max} - qpx/\varepsilon_r\varepsilon_o \text{ for } 0 < x < a \\ &= -qnx(W_{Dn}-x)/\varepsilon_r\varepsilon_o \text{ for } a < x < W_{Dn} \end{aligned} \tag{8.24}$$

where E_{max} is given as

$$E_{max} = q[-pa+n(W_{Dn}-x)]/\varepsilon_r\varepsilon_o \tag{8.25}$$

Conduction-band minimum (E_C) reaches a maximum at $x = b$, where

$$b = [ap-(W_{Dn}-x)n]/p \tag{8.26}$$

Φ_B is thus increased from Φ_B of a SBD without a thin p$^+$-type layer by

$$\Delta\Phi_B = E_{max}b - qpb^2/2\varepsilon_r\varepsilon_o \tag{8.27}$$

When p and ap are designed to be much larger than n and $W_{Dn}n$, respectively, $\Delta\Phi_B$ approaches $\Phi_B + qpa^2/2\varepsilon_r\varepsilon_o$; namely, effective Φ_B increases (Figure 8.11[c]).

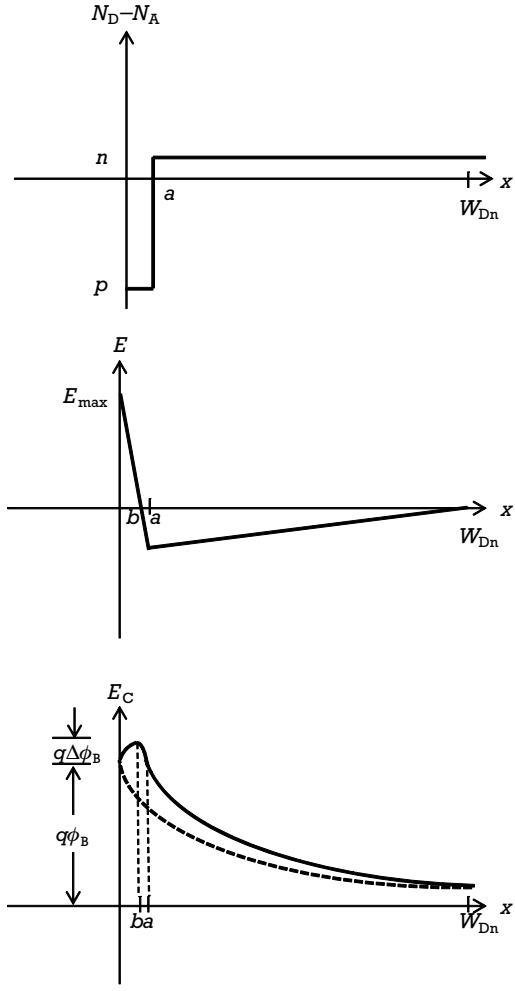

Figure 8.11 Distributions of (a) idealized profile of net donor concentration, (b) electric field, and (c) conduction-band minimum.

An SBD with a thin p^+-layer, namely, a 4H-SiC trench SBD in which the trenches extend into the p^+-type regions (Figure 9.9[d]), has been demonstrated. As simulated in the case of 0.6-kV class SBDs [43], the region where $|E|$ exceeds 1.5 MV/cm appears below the bottom of the trenches of the trench SBD, while it appears around the Schottky junction of the planar SBD (Figure 8.12). At a reverse bias of 0.6 kV, E_{max} at the Schottky junction of the trench SBD is 0.68 MV/cm, which is less than half that of the planar SBD (1.65 MV/cm) [43]. In the case of a 5-μm-thick n-type drift layer ($N_D = 1.0 \times 10^{16}$ cm^{-3}), metal with large Φ_B (e.g., 1.31V) is needed to suppress

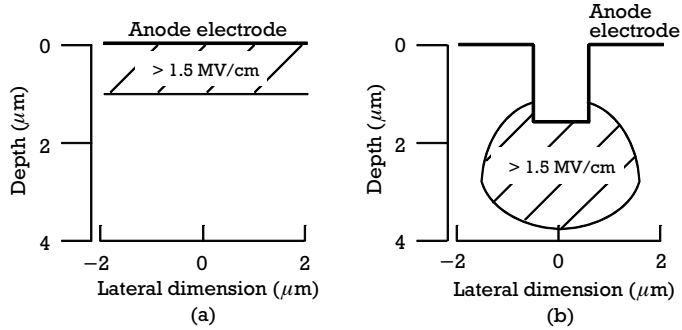

Figure 8.12 Simulated distributions of regions where electric-field strength exceeds 1.5 MV/cm in 0.6-kV reverse-biased (a) planar and (b) trench SBDs with a thin p^+-type layer [43].

reverse leakage at 0.6 kV. Owing to the combination of a thin p^+-region and a trench structure, metal with small Φ_B (0.85V) was successfully formed on the drift layer with 1.05-μm-deep trenches; namely, V_F was reduced by 0.48V, while comparable reverse leakage was kept at 0.6 kV (i.e., $< 1 \times 10^{-6}$A for a 3.06-mm^2 chip) [43].

Reported current/voltage characteristics of a 4H-SiC trench SBD with a p^+-type region [43] and a 0.79-kV pure GaN SBD [21] are shown in Figure 8.13. Under the condition of P_P = 300 W/cm^2, V_F of the 4H-SiC trench SBD with a p^+-type region (1.03V) is 0.27V lower than that of the pure GaN SBD (Figure 8.13[a]). With respect to reverse characteristics, both SBDs have practically low leakage-current-density (< 1 mA/cm^2) (Figure 8.13[b]); however, J_R at V_R = 0.7 kV of the pure GaN SBD is about six times larger than that of the 4H-SiC trench SBD with a p^+-type region. Note that although it is possible to fabricate GaN trench SBDs by using ICP etching and wet etching (Section 7.2), it is difficult to fabricate GaN trench SBDs with a thin p^+-type region due to the difficulty of increasing the activation ratio of ion-implanted magnesium acceptors (Section 7.3.1).

8.10 Shielded Planar SBDs

A shielding technique to reduce $|E|$ at the Schottky junction of trench SBDs with a thin p^+-type region has also been applied to planar SBDs by alternately forming Schottky and p-n junctions (Figure 8.9[e–g]). The shielded planar SBDs whose anode metal and p-n junctions make ohmic contacts are called merged p-n Schottky (MPS) diodes. On the other hand, the shielded planar SBDs whose anode metal and p-n junctions make Schottky contacts are called JBS diodes. Forward current flows through the Schottky junctions only in the case of MPS diodes and junction barrier Schottky (JBS)

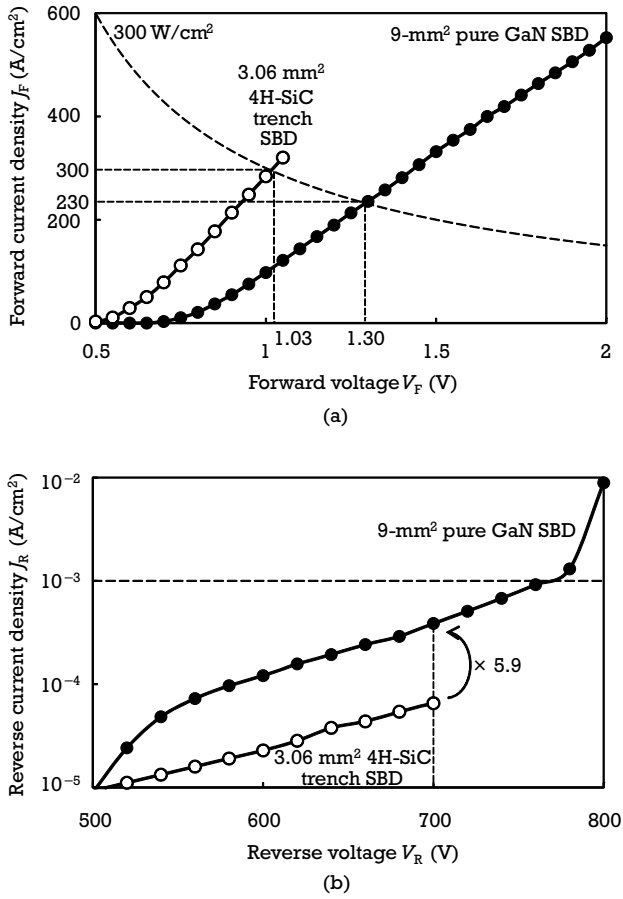

Figure 8.13 Room-temperature (a) forward and (b) reverse current-density/voltage characteristics of the reported 0.7-kV-class 4H-SiC trench SBD with a thin p^+-type layer [43] and pure SBD [21].

diodes when $V_F < E_g/q$ (Figure 8.9[e, g], respectively). In contrast, forward current also flows through the p-n junctions of MPS diodes when $V_F > E_g/q$ (Figure 8.9[f]).

The electron-hole recombination energy is known to be used often for creating defects [44] (see Section 12.6). Since the stacking-fault energy of 4H-SiC (0.014 J/m^2 [45]) is much smaller than that of GaN (1.2 J/m^2 [46]) (Section 2.2.3), a JBS diode is preferred to an MPS diode in the case of 4H-SiC diodes. With respect to shielded GaN SBDs, on the other hand, MPS diodes, in which p^+-type regions exist in the active area, are preferred because using magnesium-ion implantation in the edge-termination area is difficult.

8.10.1 GaN merged p-n Schottky diodes

GaN MPS diodes (Figure 8.9[e, f]) have been fabricated, and their current/voltage characteristics were compared with those of pure GaN SBDs and GaN p-n diodes [47]. As shown in Figure 8.14(a), the turn-on voltage of GaN MPS diodes (0.8V) agrees with that of pure GaN SBDs. Although J_F of pure GaN SBDs saturates around 4.4 kA/cm^2, J_F of GaN MPS exponentially increases due to current flow through the p-n junctions. *BV* of GaN MPS diodes is 1.6 kV, which lies between BV of pure GaN SBDs and *BV* of GaN p-n diodes (Figure 8.14[b]).

8.10.2 4H-SiC JBS Diodes

In JBS diodes, regions of p$^+$-n and Schottky junctions are alternated to shield the Schottky junction against a high electric field [48] (Figure 8.9[g]). The

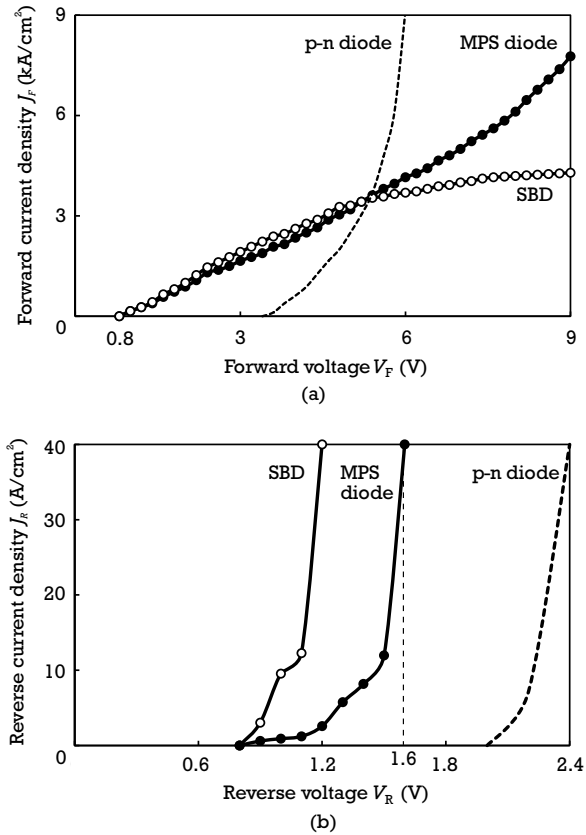

Figure 8.14 Room-temperature (a) forward and (b) reverse current-density/voltage characteristics of reported 0.01-mm^2 GaN MPS diode [47].

space between the p^+-type regions is chosen so as not to prevent unipolar conduction in the on-state. The first high-voltage SiC JBS diodes were reported in 1998 [49, 50]. *BV* of 0.7 kV was achieved with a 9-μm-thick drift layer doped at 3×10^{15} cm^{-3} [50]. *BV* of 4H-SiC JBS diodes was then improved to 2.8 kV with a 27-μm-thick drift layer doped at 3×10^{15} cm^{-3} [51], 4.3 kV with a 30-μm-thick drift layer doped at 2×10^{15} cm^{-3} [52], and 10 kV with a 120-μm-thick drift layer doped at 6×10^{14} cm^{-3} [53].

4H-SiC JBS diodes have been implanted with aluminum ion (see Section 7.3.2). J_F/V_F characteristics of these 4H-SiC JBS diodes were thus analyzed by assuming the ratio of the laterally extended length to the vertical depth of the p^+-n junction (r) to be 85% in the case of silicon JBS diodes [54] and 1.5% in the case of 4H-SiC JBS diodes [55]. The much smaller r in the latter case originates from the extremely low diffusivity of aluminum [56]. On the other hand, the vertical concentration profile of implanted aluminum in 4H-SiC results in an extended tail due to channeling (see Section 7.3.2). Furthermore, according to two-dimensional Monte Carlo simulation, implanted aluminum ions and implantation-induced point defects laterally spread from the edge of the implantation mask [57–59]. To take such effects into account is thus important when the spacing between the p^+-type regions in 4H-SiC JBS diodes is reduced. For example, 4H-SiC JBS diodes with 2-μm-wide p^+ stripe regions separated by 1 μm and nickel/4H-SiC SBDs were experimentally and computationally investigated [57]. As for an example of a 22-μm-thick drift layer doped with silicon at 3×10^{15} cm^{-3}, the measured J_F/V_F characteristics of a 1.8-mm^2 nickel/4H-SiC SBD (open circles) are reproduced with a simulation that assumes $q\Phi_B$ of 1.59 eV and a uniform μ_n of 840 cm^2/Vs (dashed line) (Figure 8.15). However,

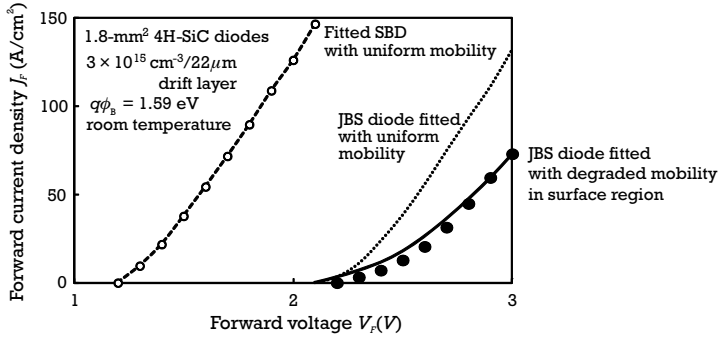

Figure 8.15 Forward-current-density/voltage characteristics of measured (symbols) and simulated (lines) nickel/4H-SiC SBD and JBS diodes with a 22-μm-thick drift layer doped at 3×10^{15} cm^{-3}. Simulation is carried out by assuming uniform μ_n of 840 cm^2/Vs (dashed and dotted lines) or degraded μ_n of 450 cm^2/Vs in the 0.23-μm-thick surface region (solid line).

when measured J_F/V_F characteristics of 1.8-mm^2 4H-SiC JBS diodes were simulated under the same assumption, J_F was overestimated (dotted line). A two-layer model taking into account the lateral spreading of implantation-induced point defects was thus proposed [57]. According to the model, since the region with significant lateral spreading of interstitials is shallower than 0.23 μm, μ_n in the surface region was considered to be degraded. The measured J_F/V_F characteristics of a 1.8-mm^2 4H-SiC JBS diode (solid circles) are successfully reproduced with a simulation that assumes μ_n of 450 cm^2/Vs in the region shallower than 0.23 μm and 840 cm^2/Vs in the region deeper than 0.23 μm (dashed line).

8.11 Summary

The first half of this chapter explains the physics of metal-semiconductor contacts, including Schottky-barrier lowering, as well as the current-transport theories based on diffusion and thermionic-emission diffusion. Compared to conventional pure SBDs, SBDs with structures with a thin p$^+$-type or wider-bandgap layer and/or with a reduced electric field are better approaches from the viewpoint of decreasing reverse leakage. The second half of this chapter introduces graded AlGaN SBDs, 4H-SiC trench SBDs with a thin p$^+$-type region, GaN MPS diodes, and 4H-SiC JBS diodes, in addition to pure GaN and 4H-SiC SBDs.

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CHAPTER

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Metal-Insulator-Semiconductor Capacitors and Unipolar Power-Switching Devices

9.1 Introduction

As described in Section 7.5.2, SiC can be thermally oxidized in the same manner as silicon, except for the simultaneous production of CO. On the other hand, a deposited SiN_x or Al_2O_3 layer is frequently used as an insulator on GaN and AlGaN (see Section 7.5.1). Therefore, in this chapter, MIS is used for GaN and SiC and metal-oxide-semiconductor (MOS) is used for silicon only.

Unipolar power-switching devices include the MISFET and the static-induction transistor (SIT) [1], which consists of a p-n-junction-gate SIT (also called a junction field-effect transistor [JFET]), a Schottky-junction-gate SIT (also called a metal-semiconductor field-effect transistor [MESFET]), and a p^+-gate SIT (also called

a p^+-gate FET). With respect to JFETs, 0.6-kV-class 4H-SiC products are commercially available; however, most of them have normally-on characteristics (Figure 9.1[a]), which are an impediment to some circuit applications [2]. Although conventional MESFETs also have normally-on characteristics, V-grooved AlGaN/GaN MESFETs were reported to exhibit normally-off characteristics (Figure 9.1[b]) [3]. Therefore, this chapter focuses on MISFETs, MESFETs, and p^+-gate FETs. A brief review of the physics of MIS capacitors is followed by an introduction to GaN heterojunction FETs (HFETs), 4H-SiC JFETs, and GaN and 4H-SiC MISFETs, including those with trenched-gate and SJ structures (see Sections 6.6 and 7.2.1).

9.2 MIS Capacitors

9.2.1 Idealized MIS Capacitors

A MIS capacitor is a capacitor formed from metal, insulator, and semiconductor layers. Although the MIS capacitor has been directly applied to, for example, charge-coupled devices for optical imaging and signal processing, it is not only the basic building block of MISFETs but also the most useful tool to study semiconductor surfaces.

Section 8.1 considers a metal/n-type semiconductor contact; in contrast, this section studies a metal/insulator (thickness: d)/p-type semiconductor structure. The structure is assumed to have no charges in the insulator and no interface states or fixed charges at the insulator/p-type semiconductor interface. (The influence of insulator and fixed charges on the MIS structure is described in the Section 9.2.2.) As described in Section 8.1, electron affinity [$q\chi_i$ for the insulator and $q\chi$ for the p-type semiconductor shown in Figure 9.2(a)] is the difference between the vacuum level

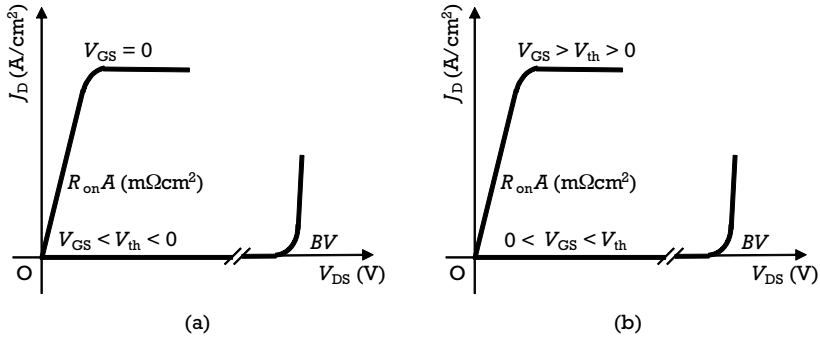

Figure 9.1 Schematic drain current-density (J_D)/drain-source voltage (V_{DS}) characteristics of (a) normally-on and (b) normally-off power-switching devices. V_{th} denotes the threshold voltage explained in Section 9.2.1.

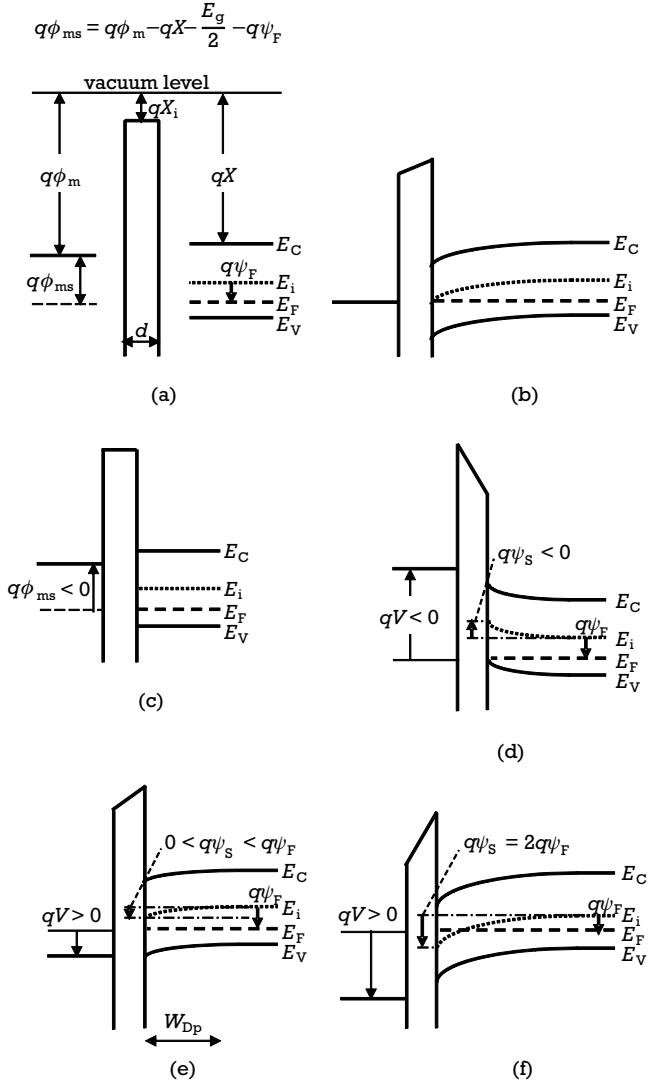

Figure 9.2 Energy-band diagrams of a metal, insulator, and p-type semiconductor when the metal work function is lower than the semiconductor work function: (a) separated, (b) connected with zero bias, and (c) connected with flat-band bias and the bias conditions of (d) accumulation, (e) depletion, and (f) inversion.

and conduction-band minimum E_C. Since the intrinsic Fermi level E_i, which is the Fermi level of an intrinsic semiconductor, lies in the middle of band-gap E_g, the work function of the p-type semiconductor, $q\Phi_s$, is expressed as

$$q\Phi_s = q\mathrm{X} + (E_g/2) + q\Psi_F \tag{9.1}$$

where Ψ_F is the Fermi potential defined as the difference between E_i/q and E_F/q and can be calculated from ionized acceptor concentration N_A^- and intrinsic carrier concentration n_i (see Section 2.4) as [4]

$$\Psi_F = (kT/q) \ln(N_A^-/ n_i) \tag{9.2}$$

When the metal work function, $q\Phi_m$, is lower than $q\Phi_s$, the energy bands bend downward [Figure 9.2(b)]. Since the difference between the work functions of a metal and a p-type semiconductor, $q\Phi_{ms}$, is given as

$$q\Phi_{ms} = q\Phi_m - q\chi - (E_g/2) - q\Psi_F \tag{9.3}$$

the flat-band condition (Figure 9.2[c]) is realized when flat-band voltage $V_{FB} = \Phi_{ms}$ (< 0) is applied to the metal, and the p-type semiconductor is grounded.

If the p-type semiconductor is held at ground and voltage V applied to the metal is kept negative but increased in magnitude above $|\Phi_{ms}|$, the surface potential Ψ_S, which is defined as the total band bending from the substrate to the surface, becomes negative [Figure 9.2(d)]. Since no current flows in the MIS structure, E_F remains flat, resulting in an accumulation of holes near the surface of the p-type semiconductor (a so-called accumulation case).

When V is positive, on the other hand, the bands bend downward. When V is so small that the condition $0 < \Psi_S < \Psi_F$ is satisfied (Figure 9.2[e]), holes are depleted from the surface of the p-type semiconductor (a so-called depletion case). Similar to (3.30), depletion width W_{Dp} is given as

$$W_{Dp} = [2\varepsilon_r\varepsilon_o\Psi_S/qN_A]^{0.5} \tag{9.4}$$

Total charge in the depletion region, Q_D, can be obtained as

$$Q_D = -qN_AW_{Dp} = -[2q\varepsilon_r\varepsilon_oN_A\Psi_S]^{0.5} \tag{9.5}$$

which is balanced by a positive sheet charge on the metal surface.

When V is large enough for E_i at the surface of the p-type semiconductor to cross over E_F, Ψ_S becomes $2\Psi_F$ (Figure 9.2[f]); namely, electron concentration at the surface of the p-type semiconductor equals hole concentration in the bulk. The voltage at which this state occurs is known as the threshold voltage V_{th}. The condition $V > V_{th}$ is called the inversion case. Once the p-type semiconductor is biased into inversion, electron concentration at the surface of the p-type semiconductor becomes an approximate exponential function of Ψ_S, which thus changes little with increasing V. As

a result, W_{Dp} and total potential drop across the depletion region ($2\phi_F$) are relatively constant.

9.2.2 Influence of Insulator and Fixed Charges on MIS Capacitors

The effect of insulator charge is first treated one-dimensionally [5]. The case that a density of charge Q_I is located on plane $x = x_I$ ($0 \le x_I \le d$) is considered, as shown in Figure 9.3(a). The charge at x_I induces equal and opposite charges that are divided between the p-type semiconductor and the metal. A shift in V_{FB} (ΔV_{FB}) can be obtained by using Gauss's law as follows. The constant electric field E_I between the metal ($x = 0$) and Q_I ($x = x_I$) (Figure 9.3[b]) is given as

$$E_I = -Q_I/\varepsilon_I\varepsilon_o \tag{9.6}$$

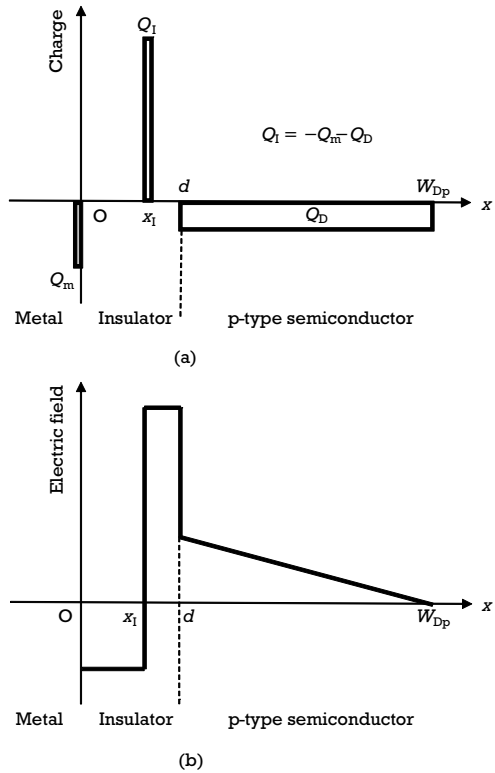

Figure 9.3 Schematic illustrations for analyzing the effect of an insulator-charge density Q_I on MIS structure. (a) Charge configuration at zero bias ($Q_I = -Q_m - Q_D$) and (b) electric-field distribution at zero bias.

where ε_I is the relative permittivity of the insulator. ΔV_{FB} is thus obtained as

$$\Delta V_{FB} = x_I E_I = -x_I Q_I / \varepsilon_I \varepsilon_o \tag{9.7}$$

Since insulator capacitance per unit area (C_I) is given as

$$C_I = \varepsilon_I \varepsilon_o / d \tag{9.8}$$

(9.7) can be expressed as

$$\Delta V_{FB} = -x_I Q_I / C_I d \tag{9.9}$$

which reaches a maximum when $x_I = d$.

The above equations can be generalized for ΔV_{FB} by an arbitrary distribution of charge $\rho(x)$ by superimposing and integrating the increments that result from charges distributed throughout the insulator as follows:

$$\Delta V_{FB} = -\left(1 / C_I\right) \int_0^{x_I} \left(x / x_I\right) \rho(x) dx \tag{9.10}$$

In contrast, fixed charge at the insulator/p-type semiconductor interface (Q_f) contributes to ΔV_{FB} through $-Q_f/C_I$. Therefore, V_{FB}, which includes the effects of Φ_{ms}, insulator charge, and interface charge, can be written as

$$\Delta V_{FB} = \Phi_{ms} - \left(1 / C_I\right) \int_0^{x_I} \left(x / x_I\right) \rho(x) dx - Q_f / C_I \tag{9.11}$$

9.3 AlGaN/GaN Heterostructures

Distribution of conduction-band edge E_C of a typical AlGaN/GaN heterostructure formed on GaN (0001) is shown in Figure 9.4(a). Both spontaneous and piezoelectric polarizations are known to induce charges in this material system [6]. The wider bandgap of AlGaN creates a conduction-band discontinuity, ΔE_C, which leads to formation of a two-dimensional electron gas (2DEG). As described in Section 8.8, oxygen-related shallow donors (e.g., with energy depth E_{SD} of 0.03 eV [7, 8] for $Al_{0.26}Ga_{0.74}N$) exist on the AlGaN surface, so the Fermi level is pinned at E_{SD}. On the AlGaN surface, polarization charge $-\sigma_{AlGaN}$ balances qN_{SD}^+, where N_{SD}^+ is ionized surface-donor concentration (Figure 9.4[b]). Since at the AlGaN/GaN interface, 2DEG charge $-\sigma_{2DEG}$ and polarization charge $-\sigma_{GaN}$ balance polarization charge $+\sigma_{AlGaN}$, σ_{2DEG} is given as

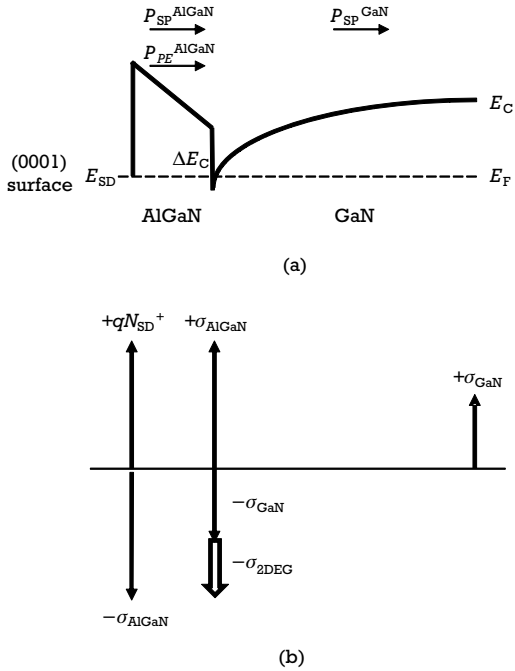

Figure 9.4 Distribution of (a) conduction-band edge and (b) interface charges of a typical AlGaN/GaN heterostructure formed on GaN (0001). (P_{SP}: spontaneous polarization; P_{PE}: piezoelectric polarization.)

$$\sigma_{2DEG} = \sigma_{AlGaN} - \sigma_{GaN} \tag{9.12}$$

Sheet-electron concentration n_s and electron mobility μ_n of a 2DEG formed on GaN (0001) and Si (111) substrates were measured [9]. While $n_s^{GaN(0001)}$ was similar to $n_s^{Si(111)}$ (5.6–5.7 × 10^{12} cm^{-2}), $\mu_n^{GaN(0001)}$ (1,900 cm^2/Vs) was 30% larger than $\mu_n^{Si(111)}$ (1,450 cm^2/Vs) due to improved GaN crystal quality. This 2DEG sheet resistance, $\rho_{2DEG}^{GaN(0001)}$, of 580 Ω/sq is used for estimating specific on-resistance $R_{on}A$ in Section 9.5.1.

9.4 Band Lineup for GaN, AlN, 4H-SiC, and Representative Insulators

Figure 9.5, based on [10–14], summarizes a band lineup for GaN, AlN, 4H-SiC, and representative insulators. With respect to an insulator for GaN MIS capacitors, SiN_x [15], Al_2O_3 [16, 17], and HfO_2 [18] have been adopted. It was reported that high-density mid-gap states existed at the Al_2O_3/(Al)GaN interface [19] probably due to Ga–O bond formation [20]. To reduce the influence of such Ga–O bond formation, in-situ NH_3-plasma treatment [21],

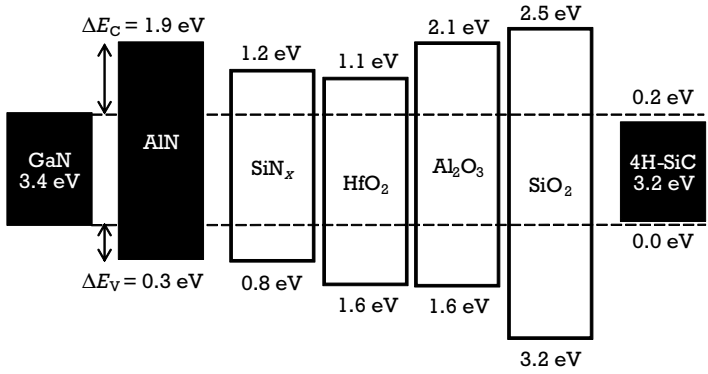

Figure 9.5 Band lineup for GaN, AlN, 4H-SiC, and representative insulators [10–14].

in-situ MOCVD-grown thin AlN layers [22, 23] and atomic-layer-deposited AlN layers [24] have been investigated.

9.5 GaN HFETs

A GaN HFET is a GaN FET in which a layer of wider-bandgap material (i.e., AlGaN) is epitaxially grown over a 2DEG channel. It is also known as a GaN HEMT because of the high electron mobility of a 2DEG (see Section 9.3). The wider-bandgap material can be used as a part of multiple insulator layers (i.e., GaN MIS HFETs—see Section 9.5.1) or as a single insulator layer (i.e., GaN MESFETs and GaN p^+-gate HFETs—see Sections 9.5.2 and 9.5.3).

9.5.1 GaN MIS HFETs

In GaN MISFETs, an insulator layer is formed on an AlGaN layer to suppress gate leakage current. A schematic cross-sectional view of the first vertical GaN MIS HFET on a freestanding GaN substrate is shown in Figure 9.6 [25]. Electron current flows through the AlGaN/GaN heterojunction and the aperture, spreads into the drift layer at about a 45-degree angle, and finally becomes uniform. During the off-state, the p^+-GaN region plays the role of a current-blocking region. According to (3.25), sheet concentration of acceptors in the depleted p^+-GaN region is equal to sheet concentration of donors in the depleted n-GaN drift layer. Even when the depleted n-GaN width equals the thickness of n-GaN drift layer (t_{drift}), the depleted p^+-GaN width must be less than the thickness of the p^+-GaN region (t_{p+}) to prevent a phenomenon called punch-through. This condition was satisfied in [25] because sheet-acceptor concentration (3×10^{14} cm^{-2}) in the p^+-GaN region was much larger than sheet-donor concentration (3×10^{12} cm^{-2}) in the

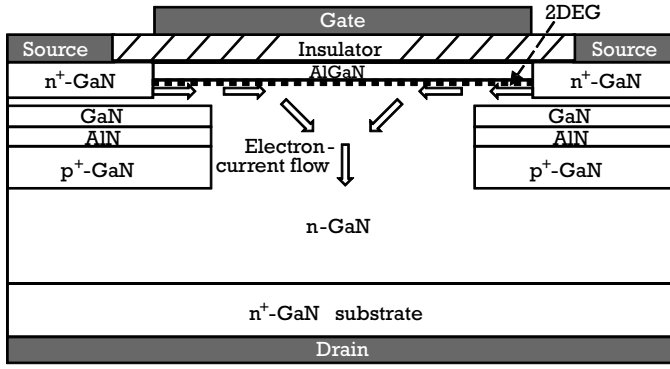

Figure 9.6 Schematic cross-sectional view of the first vertical GaN MIS HFET on a free-standing GaN substrate [25].

n-GaN drift layer as long as all the doped magnesium and silicon atoms became, respectively, acceptors and donors. Breakdown voltage *BV* (Figure 9.1) can then be determined as the voltage at which the maximum electric field at the p^+/n GaN junction (E_{max} in Section 3.5) equals the critical electric field ($E_{critical}$ in Section 2.6). However, *BV* was not reported in [25].

The process flow for forming the aperture in Figure 9.6 is shown in Figure 9.7. A 3-μm-thick n-GaN layer, a 0.1-μm-thick p^+-GaN layer, a 10-nm-thick AlN layer, and a 50-nm-thick GaN layer were grown on an n^+-GaN (0001) substrate by MOCVD (see Section 6.2) (Figure 9.7[a]). The GaN/AlN/p^+-GaN layer was dry-etched by ICP dry etching with Cl_2 gas and an SiO_2 mask (see Section 7.2.1) (Figure 9.7[b]). After the mask was removed, a 0.3-μm-thick n-GaN layer (Si: 1×10^{16} cm^{-3}) and a 15-nm-thick $Al_{0.25}Ga_{0.75}N$ layer were grown by MOCVD (Figure 9.7[c]). Here, the AlN layer was used to suppress mass transport from the surface to the aperture region [26].

Silicon-ion implantation was used to form n^+-GaN source regions (see Section 7.3.1). As a gate insulator and an electrode, a 50-nm-thick high-temperature SiO_2 layer and a 250-nm-thick phosphorous-doped polycrystalline silicon film were deposited by low-pressure chemical vapor deposition. Annealing to activate the polycrystalline silicon (at 850°C for 20 min) also activated hydrogenated magnesium [27]. It should be noted here that magnesium in the p^+-GaN on which n-GaN is grown is not fully dehydrogenated by activation annealing [28]; therefore, ammonia-molecular beam epitaxy, instead of MOCVD, was recently used to fabricate GaN MIS HFETs without activation annealing [29].

In [25], the source and drain electrodes made of titanium (20 nm)/aluminum (1 μm) were formed by electron-beam evaporation. The GaN MIS

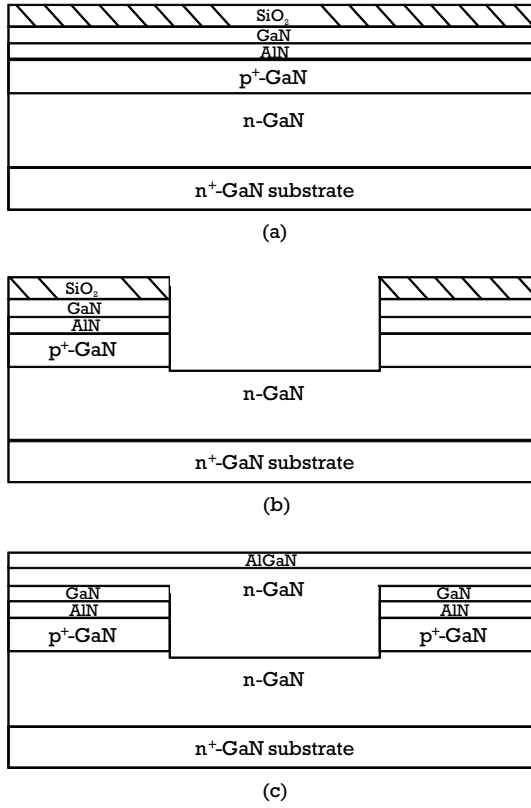

Figure 9.7 Process flow for fabricating the aperture shown in Figure 9.6 [25].

HFET had normally-on characteristics with V_{th} of −16V. At gate-source voltage V_{GS} of 0V, $R_{on}A$ was 2.6 mΩcm^2, which can be further reduced by decreasing the width of the JFET region, W_{JFET} (Figure 9.8), as explained next.

$R_{on}A$ is ideally determined by the specific resistance of the components in the current path shown in Figure 9.8:

$$R_{on}A = R_S A + R_{ch}A + R_{accum}A + R_{JFET}A + R_{drift}A + R_{sub}A \tag{9.13}$$

where $R_S A$ is specific source resistance, $R_{ch}A$ is specific channel resistance, $R_{accum}A$ is specific accumulation-region resistance, $R_{JFET}A$ is specific JFET-region resistance, $R_{drift}A$ is specific drift-region resistance, and $R_{sub}A$ is specific substrate resistance (see Section 1.3.1). In (9.13), $R_S A$ can be neglected because source regions are usually heavily doped. $R_{ch}A$ is given as

$$R_{ch}A = \rho_{2DEG}{}^{GaN(0001)}\, L_{ch}\, (P/2), \tag{9.14}$$

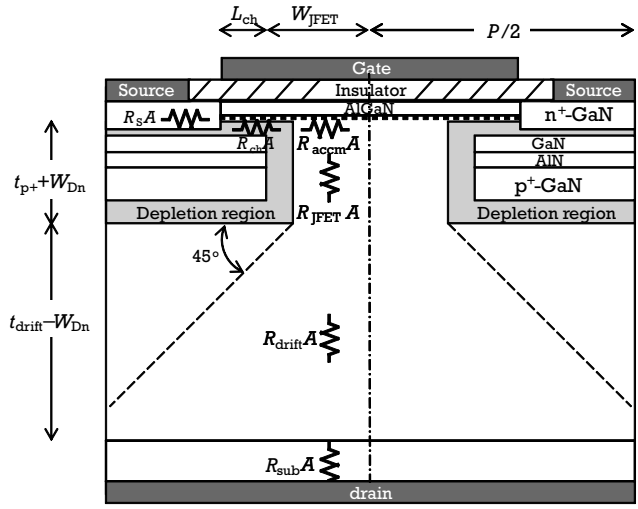

Figure 9.8 Specific resistances in the current flow path of the vertical GaN MIS HFET shown in Figure 9.6.

where L_{ch} is channel length and P is cell pitch (Figure 9.8). $R_{ch}A$ can be approximated as

$$R_{accum}A = 0.6\,\rho_{2DEG}{}^{GaN(0001)}\,W_{JFET}\,(P/2) \tag{9.15}$$

where the factor 0.6 is typically used for vertical silicon power-switching devices to account for two-dimensional current spreading from the channel into the JFET region [30]. $R_{JFET}A$, $R_{drift}A$, and $R_{sub}A$ are expressed as

$$R_{JFET}A = \rho_{drift}\,(t_{p+}+W_{Dn})(P/2)/(W_{JFET}-W_{Dn}) \tag{9.16}$$

$$\begin{aligned} R_{drift}A = \rho_{drift}\{&[(P/2)\ln[(P/2)/(W_{JFET}-W_{Dn})] \\ &+ t_{drift}-W_{Dn}-[(P/2)-W_{JFET}]\} \end{aligned} \tag{9.17}$$

$$R_{sub}A = \rho_{sub}\,t_{sub} \tag{9.18}$$

where ρ_{drift} is resistivity of the drift region, ρ_{sub} is resistivity of the substrate, t_{sub} is thickness of the substrate, and depleted n-GaN width W_{Dn} is already given as (3.30); namely,

$$W_{Dn} \approx (2\varepsilon_r\varepsilon_o\Psi_{bi}/qN_D)^{0.5} \tag{9.19}$$

Note that in (9.13), specific contact resistance is neglected due to its small value (i.e., 8×10^{-5} Ωcm^2) [25]. Built-in potential Ψ_{bi} is given as [31]

$$\Psi_{bi} = (kT/q) \ln(N_A N_D / n_i^2), \tag{9.20}$$

where n_i^{GaN} is already given as (2.7a); namely,

$$n_i^{GaN} = 2.0\times10^{15} T^{1.5} \exp(-2.0\times10^4/T) \text{ (cm}^{-3}) \tag{9.21}$$

In the case $P/2 = W_{JFET} + 4\ \mu$m, $R_{on}A$ of the vertical GaN MIS HFET at 300K is calculated as a function of W_{JFET} (Figure 9.9). In [25], $L_{ch} = 2\ \mu$m and $W_{JFET} = 1.5\ \mu$m. Other parameters used to calculate the curves in Figure 9.9 are listed as follows: $\rho_{2DEG}^{GaN(0001)} = 580$ Ω/sq (Section 9.3); $\mu_n = 850$ cm^2/Vs (Figure 2.16); $\varepsilon_r = 10.4$ [32]; $\rho_{sub} = 0.018$ Ωcm and $t_{sub} = 600\ \mu$m [33]. Calculated $R_{on}A$ reaches a minimum of 1.7 mΩcm^2 at $W_{FET} = 3.5\ \mu$m. $R_{accum}A$ increases with W_{JTEF} when $W_{JFET} < 3.5\ \mu$m, while contributions of $R_{drift}A$ and $R_{JFET}A$ become large when $W_{JFET} > 3.5\ \mu$m. Since the contribution of $R_{sub}A$ (i.e., 1.1 mΩcm^2) is dominant, in the present case of a 3-μm-thick 1×10^{16}-cm^{-3} doped n-GaN drift layer, thinning GaN substrates is effective for reducing $R_{on}A$.

Note that in contrast to the above-described epitaxially grown p$^+$-type GaN buried regions [25], magnesium-ion-implanted p$^+$-type GaN buried regions have also been used [34]. Activation annealing was carried out at 1,553K in NH_3+N_2 ambient, and the resultant BV and $R_{on}A$ were 250V and 2.2 mΩcm^2, respectively.

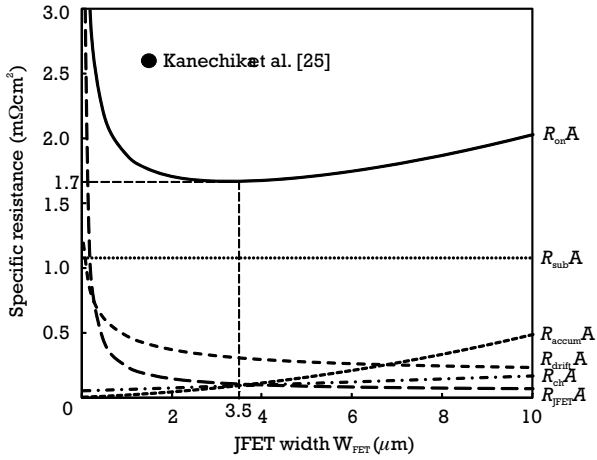

Figure 9.9 Specific resistance of a vertical GaN MIS HFET (Figure 9.6) as a function of JFET width calculated from (9.13) to (9.21) in the case $P/2 = W_{JFET} + 4\ \mu$m.

9.5.2 GaN MESFETs

In GaN MESFETs, no insulator layers are formed on an AlGaN layer. As shown in Figure 9.10, the direction of spontaneous polarization is parallel to a GaN $(11\bar{2}0)$ surface. Since only piezoelectric polarization induces charges at the AlGaN/GaN interface formed on GaN $(11\bar{2}0)$, n_s becomes smaller than that at the AlGaN/GaN interface formed on GaN (0001). If the AlGaN/GaN interface is formed on a face between (0001) and $(11\bar{2}0)$, n_s takes a value between $n_s^{(0001)}$ and $n_s^{(11\bar{2}0)}$. A 0.2-μm-thick n^+-GaN layer (Si: 3×10^{18} cm^{-3}), a 1-μm-thick p^+-GaN layer (Mg: 5×10^{18} cm^{-3}), and a 5-μm-thick n-GaN layer (Si: 7×10^{15} cm^{-3}) layer were grown on an n^+-GaN (0001) substrate by MOCVD [3]. V-grooves in the n^+-GaN/p^+-GaN/n-GaN layers (with a slope angle of 16°) were formed by ICP dry etching, and $Al_{0.25}Ga_{0.75}N$/75-nm-thick GaN layers were regrown (Figure 9.11). By thinning the $Al_{0.25}Ga_{0.75}N$ layer from 35 to 10 nm, V_{th} shifted from −3.2 to +0.3V. As for the normally-on devices, BV of 672V and $R_{on}A$ of 7.6 mΩcm^2 were reported; however, neither BV nor $R_{on}A$ were reported for normally-off devices.

9.5.3 GaN p^+-gate HFETs

In GaN p^+-gate HFETs, a p^+-type GaN layer is formed on an AlGaN layer. With an appropriately designed p^+-type GaN layer, the potential of the heterojunction is lifted up only below the gate, which leads to positive V_{th} (solid line in Figure 9.12).

A 15-μm-thick n-type GaN drift layer doped at 1×10^{16} cm^{-3} was grown on an n^+-type GaN substrate (Figure 9.13[a]) and the resultant BV and $R_{on}A$ were, respectively, 1.5 kV and 2.2 mΩcm^2; however, V_{th} was relatively low (namely, 0.5V) [35].

As a function of surface tilt angle from (0001), n_s of p^+-GaN/AlGaN/GaN was calculated [36] (Figure 9.14). Reduction of n_s increased V_{th} to 2.5V

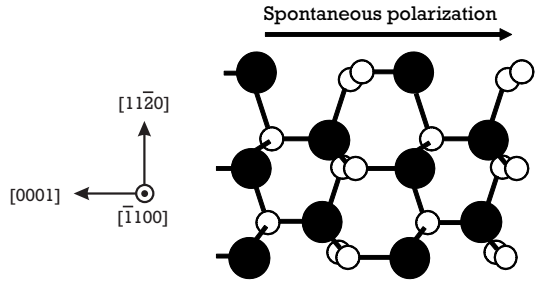

Figure 9.10 Schematic cross-section of GaN $(11\bar{2}0)$ showing direction of spontaneous polarization (solid circles: gallium atoms; open circles: nitrogen atoms).

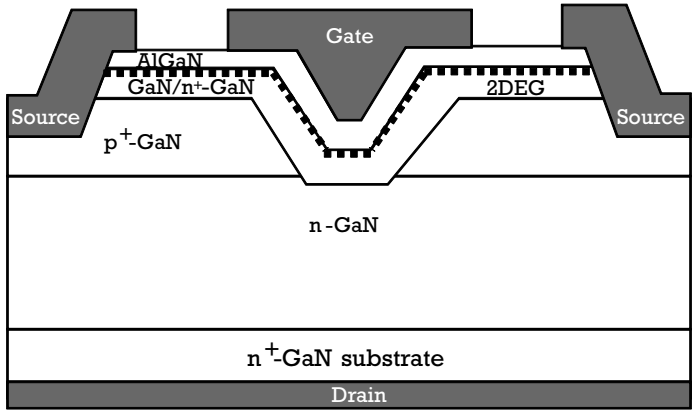

Figure 9.11 Schematic cross-sectional view of a vertical GaN MESFET on a freestanding GaN substrate [3].

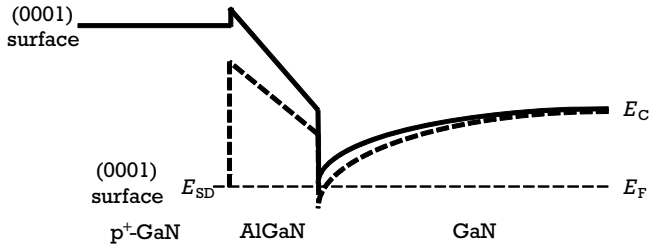

Figure 9.12 Distributions of conduction-band edge of p+-GaN/AlGaN/GaN (solid line) and AlGaN/GaN (dashed line) heterostructures formed on GaN (0001) at a gate-source bias of 0 V.

when p+-GaN/AlGaN/GaN layers were regrown over V-shaped grooves formed over an n-type GaN drift layer. On the basis of this finding, p+-GaN/AlGaN/GaN layers were regrown over the V-grooves at the surface of p+-GaN (Mg: 3×10^{19} cm^{-3}) and 13-μm-thick n-GaN (Si: 1×10^{16} cm^{-3}) drift layers by MOCVD (Figure 9.13[b]). An insulating GaN layer doped with carbon at 5×10^{18} cm^{-3} was also inserted to block off-state leakage current. After selective etchings of p+-GaN to form the gate and of AlGaN/GaN/carbon-doped GaN to form the source electrode by ICP dry etching, titanium/aluminum source and palladium/gold gate electrodes were formed on the front side, and a titanium/aluminum/titanium/gold drain electrode was formed on the backside. The resultant BV and $R_{on}A$ were, respectively, 1.7 kV and 1.0 mΩcm^2. Stable gate characteristics and successful 400-V/15-A fast switching were also demonstrated.

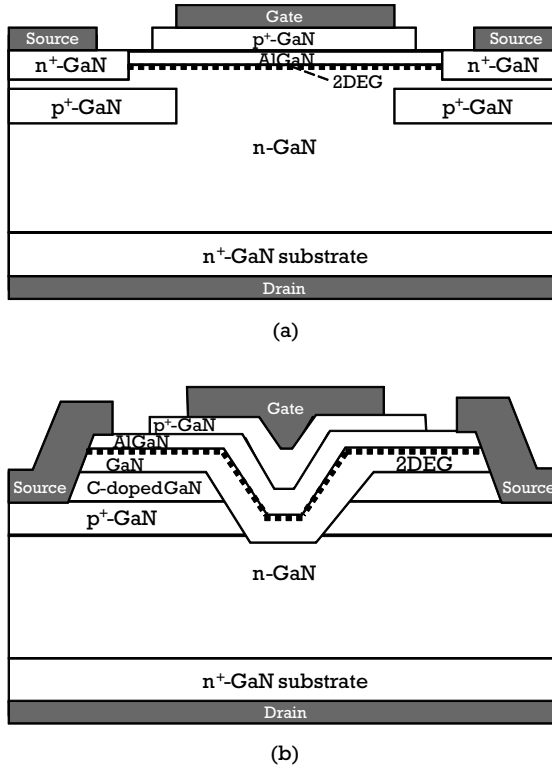

Figure 9.13 Schematic cross-sectional views of (a) planar [35] and (b) V-grooved [36] GaN p^+-gate HFETs on freestanding GaN substrates.

9.6 4H-SiC JFETs

A JFET is a buried-channel FET and is thus free from surface effects. However, the large distance between the gate and the channel makes achieving normally-off characteristics challenging (see Section 9.1). Normally-off 4H-SiC JFETs based on a trenched-and-implanted vertical channel structure (Figure 9.15[a]) were demonstrated with $R_{on}A$ of 3.6 mΩcm^2 and BV of 1.7 kV [37] and $R_{on}A$ of 130 mΩcm^2 and BV of 11 kV [38]. However, narrow channel widths (less than 1.7 μm [37] and 0.55 μm [38]) pose stringent requirements on lithography. By inserting p^+ screen grids between the gate and the drain, $R_{on}A$ of 2.4 mΩcm^2 and BV of 1.4 kV were achieved, but V_{th} was as low as +1.0V [39].

A 4H-SiC JFET with buried p^+ grids as the controlling gate (Figure 9.15[b]) was also demonstrated with $R_{on}A$ of 1.0 mΩcm^2 [40]. However, BV of 700V was measured at $V_{GS} = -12$V, which is the normally-on feature.

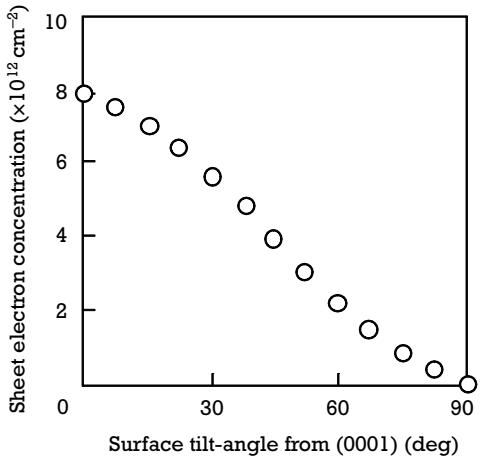

Figure 9.14 Calculated sheet electron concentration of a p^+-GaN/AlGaN/GaN channel as a function of surface tilt-angle from (0001) [36].

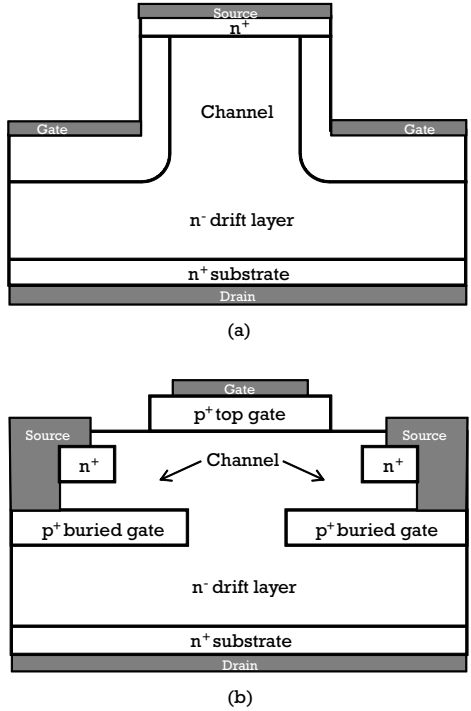

Figure 9.15 Schematic cross-sectional views of 4H-SiC JFETs with (a) trenched-and-implanted channels and (b) p^+ buried gates.

When a high-voltage normally-on 4H-SiC JFET was cascoded with a low-voltage normally-off silicon MOSFETs, the JFET-MOSFET pair operate as a normally-off power-switching device from an external perspective (Figure 9.16) [41]. A 3.3-kV normally-on 4H-SiC JFET was recently cascoded with a 80-V normally-off silicon MOSFET, and a blocking voltage higher than 4.0 kV and a low $R_{on}A$ of 14.7 mΩcm^2 were realized [42].

9.7 MISFETs

A MISFET is an FET that includes a MIS capacitor, a drift layer, and source and drain regions. The gate structure in the MIS capacitor is divided into planar and trench types, while the drift-layer structure is divided into conventional n- and SJ types. Figure 9.17(a–c) shows schematic cross-sectional views of planar, trench, and SJ MISFETs. Planar Si MOSFETs were the first unipolar power-switching devices to be commercially successful. To reduce fabrication cost, channels in these devices were formed by the so-called double-diffusion process; namely, the difference between lateral diffusivities of p- and n-type dopants defines the channels. In the cases of GaN and

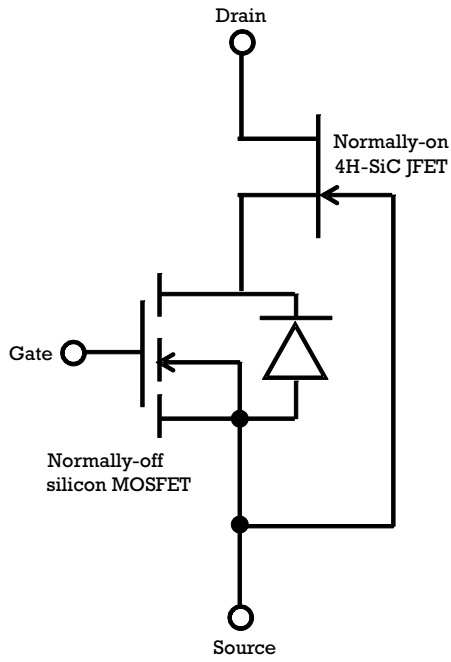

Figure 9.16 A high-voltage normally-on 4H-SiC JFET cascoded with a low-voltage normally-off silicon MOSFET.

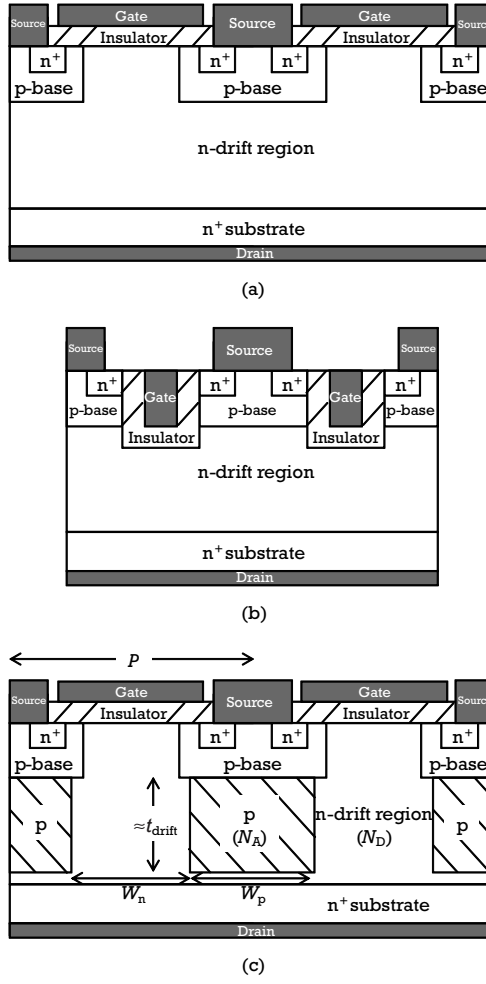

Figure 9.17 Schematic cross-sectional views of (a) planar, (b) trench, and (c) SJ MISFETs.

4H-SiC MISFETs, on the other hand, the double-diffusion process cannot be used due to lack of dopant diffusion (e.g., silicon and magnesium in GaN and aluminum in 4H-SiC) and complicated dopant diffusion (e.g., boron in 4H-SiC) (see Section 7.4). GaN and 4H-SiC planar MISFETs have therefore been fabricated by epitaxial growth and/or ion implantation.

Trench MISFETs (also called UMISFETs due to the U-shaped cross section of the gate insulator) (Figure 9.17[b]) can increase channel density because the MIS channel is oriented perpendicular to the surface. Moreover, trench MISFETs can eliminate $R_{JFET}A$ compared to planar MISFETs, resulting in extremely low $R_{on}A$ [43].

The concept of SJ devices [44], in which alternating p- and n-type columns are located in a drift layer, was first applied to a varactor diode [45], and then to commercial production of silicon SJ MOSFETs [46]. Although Figure 9.17(c) shows a planar SJ MISFET, a trench SJ MISFET can also be fabricated.

9.7.1 Planar MISFETs

To the author's knowledge, no planar GaN MISFETs have been reported. In the case of SiC, a planar 6H-SiC MISFET was fabricated in 1997 [47] using the double-implantation process, in which multiple-energy boron ions are implanted to form 1-μm-deep p-base regions (Figure 9.17[a]). The insulator used in the MIS structure was a thermally grown oxide, and inversion-layer channel mobility μ_{inv} was 20 cm^2/Vs. The reported BV and $R_{on}A$ were 760V and 130 mΩcm^2, respectively.

In 2001, a planar 4H-SiC MISFET was fabricated using a deposited oxide [48]. The reported μ_{inv}, BV, and $R_{on}A$ were 14 cm^2/Vs, 2 kV, and 55 mΩcm^2, respectively. With respect to BV and $R_{on}A$, improved values, such as 2.4 kV and 42 mΩcm^2 [49] and 10 kV and 236 mΩcm^2 [50], had been reported by 2004. In 2015, an amelioration of $R_{ch}A$ of a planar 4H-SiC MISFET was demonstrated, in which trenches were formed in the channel region to increase the channel density per area [51].

On the other hand, μ_{inv} has been increasing over time (up to, for example, 130 cm^2/Vs [52]) by improving MIS interface quality by using nitrogen [53] (see Section 7.5.2) or phosphorus [54, 55] doping during post-oxidation; strontium- [56], barium- [57], antimony- [58], or lanthanum- [52] passivation of interface-charge traps, and diffusing boron-passivation of dangling bonds in dry oxide [59, 60]. μ_{inv}-limiting factors include Coulomb scattering, surface scattering, and phonon scattering [61]; in the case of a SiO_2/4H-SiC interface, Noguchi et al. experimentally observed phonon-limited μ_{inv} and concluded that surface roughness is not the dominant μ_{inv}-limiting factor at high voltages [62].

When V_{GS} exceeds V_{th}, the surfaces of p-base and JFET regions correspond, respectively, to the inversion and accumulation cases (Section 9.2.1). Electron current flows through the inversion-layer channel (created on the surface of the p-base regions) into the accumulation layer (formed on the surface of the JFET region), spreads into the drift layer at about a 45-degree angle, and finally becomes uniform (Figure 9.18[a]). To reduce $R_{JFET}A$, heavily-doped n-type JFET regions and a current-spreading layer (CSL) (Figure 9.18[b]) have been used [63]. When such a structure is used, $R_{on}A$ of a planar 4H-SiC MISFET is ideally determined by the specific resistance of the components in the current path (shown in Figure 9.18[b]) as

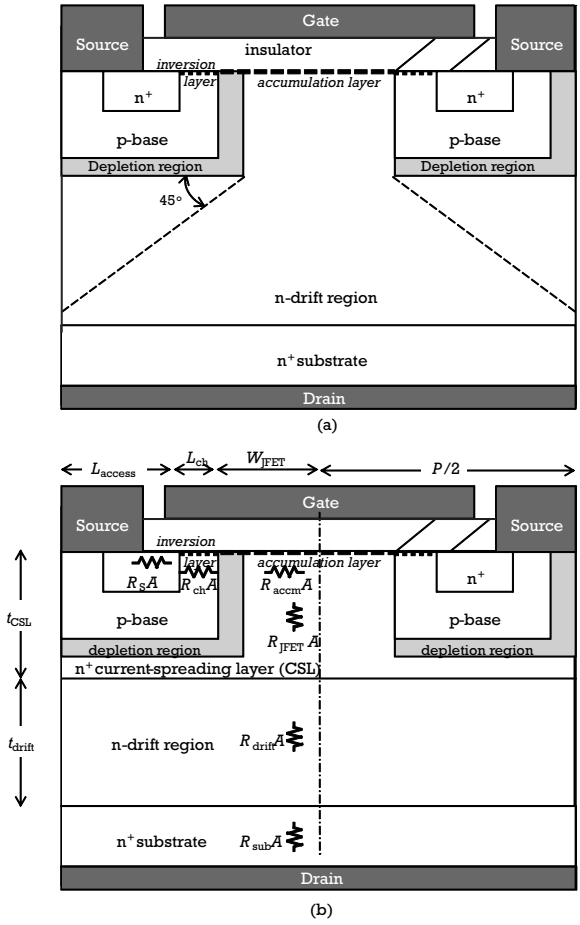

Figure 9.18 (a) Current-flow path of a planar 4H-SiC MISFET without a CSL and (b) specific resistances in the current flow path of a planar 4H-SiC MISFET with a CSL.

$$R_{on}A = R_S A + R_{ch}A + R_{accum}A + R_{JFET}A + R_{drift}A + R_{sub}A \tag{9.22}$$

In (9.22), $R_S A$ can be neglected because source regions are usually heavily doped. $R_{ch}A$ is given as

$$R_{ch}A = L_{ch}\,(P/2)/[\mu_{inv}C_I(V_{GS}-V_{th})] \tag{9.23}$$

where C_I is specific capacitance of the gate insulator, which is expressed as the ratio of the permittivity to thickness of the gate insulator; namely,

$$C_I = \varepsilon_I / t_I \tag{9.24}$$

$R_{accum}A$ is given as

$$R_{accum}A = 0.6(W_{JFET}-W_{Dn})(P/2)/[\mu_{accum}C_I(V_{GS}-V_{th})] \quad (9.25)$$

where μ_{accum} is electron mobility in the accumulation layer. Here, the factor of 0.6, which already appeared in (9.15), is typically used for vertical silicon power-switching devices to account for two-dimensional current spreading from the channel into the JFET region [30]. And W_{Dn} is obtained using (2.7b),

$$n_i^{4H\text{-}SiC} = 3.9 \times 10^{15} T^{1.5} \exp(-1.9\times10^4/T)\ (cm^{-3}) \quad (9.26)$$

and (9.19) and (9.20). $R_{JFET}A$ and $R_{drift}A$ can be approximated, respectively, as

$$R_{JFET}A = \rho_{CSL}\, t_{CSL}(P/2)/(W_{JFET}-W_{Dn}) \quad (9.27)$$

and

$$R_{drift}A = \rho_{drift}\, t_{drift} \quad (9.28)$$

where ρ_{CSL} and t_{CSL} are resistivity and thickness of the CSL. $R_{sub}A$ is given by (9.18).

In the case of the double-self-aligned short-channel 4H-SiC planar 1-kV-class MISFET reported in [64], L_{ch} = 0.5 μm; $P/2$ = 4 μm; t_I = 50 nm; W_{JFET} = 0.5 μm; $N_{CSL} = 1.0 \times 10^{17}$ cm^{-3}; t_{CSL} = 0.9 μm; $N_{drift} = 8.55 \times 10^{15}$ cm^{-3}; and t_{drift} = 8.4 μm, and $V_{GS}-V_{th}$ = 20V. With the assumption of $\mu_{accum} = \mu_{inv}$, μ_{CSL} = 600 cm^2/Vs, μ_{drift} = 850 cm^2/Vs (Figure 2.16), ρ_{drift} = 0.02 Ωcm [65], and t_{drift} = 350 μm [65], $R_{on}A$ at 300K is calculated as a function of μ_{inv} (Figure 9.19). $R_{JFET}A$ is negligibly small due to the use of a CSL. Although μ_{inv} was not described in [64], the result in Figure 9.19 indicates that in the case of 4H-SiC planar 1-kV-class MISFETs, the measured $R_{on}A$ of 6.7 mΩcm^2 [64] should decrease with increasing μ_{ch}.

With respect to higher-voltage 4H-SiC planar MISFETs, typical thickness/donor concentration in drift layers for BV of 1.7, 3.3, and 4.5 kV are, respectively, 15 μm/2 $\times$ 10^{15} cm^{-3}, 34 μm/1.5 $\times$ 10^{15} cm^{-3}, and 40 μm/1 $\times$ 10^{15} cm^{-3} [66]. Under the assumption of μ_{drift} of 850 cm^2/Vs (Figure 2.16) for the three doping levels, $R_{on}A$'s at 300K are calculated as a function of μ_{inv} (Figure 9.20). Since $R_{drift}A$ dominates $R_{on}A$ in such high-voltage MISFETs, decreasing μ_{inv} is not so important in terms of reducing $R_{on}A$.

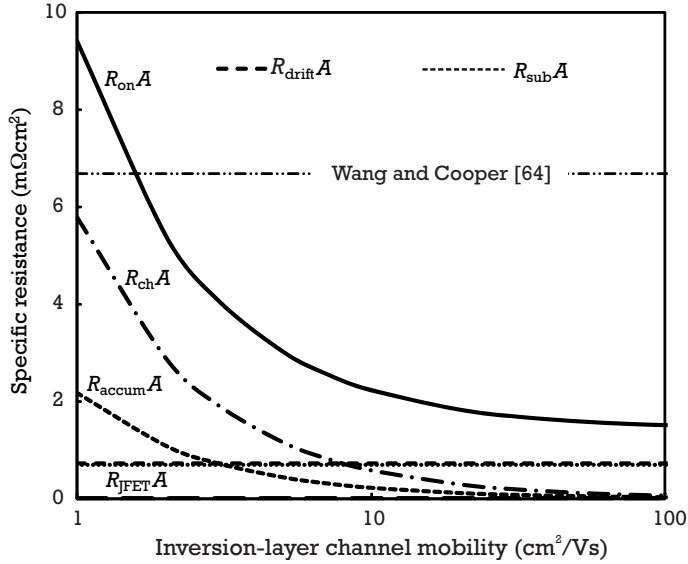

Figure 9.19 Specific resistance of a 4H-SiC planar 1-kV-class MISFET with a CSL (Figure 9.16[b]) as a function of inversion-layer channel mobility calculated from (9.18) to (9.20) and (9.22) to (9.28).

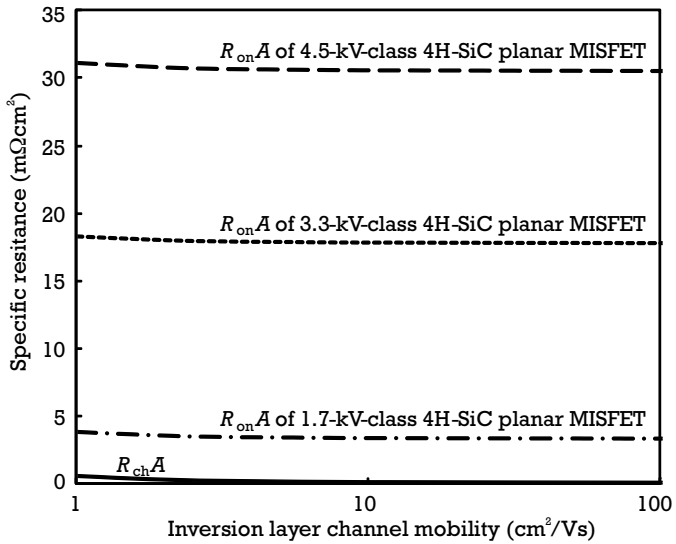

Figure 9.20 Specific resistance of 4H-SiC planar 1.7–4.5-kV-class MISFETs with a CSL (Figure 9.18[b]) as a function of inversion-layer channel mobility calculated from (9.18) to (9.20) and (9.22) to (9.28).

9.7.2 Trench MISFETs

The basic structure of a trench MISFET is shown in Figure 9.17(b). Since the first Si trench MOSFET was reported in 1985 [43], it took 11 and 23 years, respectively, for the first 4H-SiC [67] and GaN [68] trench MISFETs to be reported.

9.7.2.1 GaN Trench MISFETs

Reported values of BV and $R_{on}A$ of GaN trench MISFETs on freestanding GaN substrates are listed in Figure 9.21 [68–76]. With respect to gate layout, the use of a regular hexagonal-trench gate with a cell pitch of 12.6 μm (Figure 9.22) resulted in a ratio of gate width to unit cell area (W_G/S_{cell}) of 0.267 μm^{-1} [71], which was twice as large as W_G/S_{cell} of a stripe layout with a cell pitch of 15 μm [70]. The hexagonal layout with a cell pitch of 18 μm for a 1.5 × 1.5-mm^2 chip (active area: 1.8 mm^2) resulted in large current (23.2A) and fast switching characteristics [72]. However, μ_{inv} in an inverted p-GaN channel of conventional trench MISFETs is low. To increase electron mobility in channels, in situ oxide, GaN interlayer-based vertical trench MOSFET (OG-FET) [73, 74] and GaN vertical fin power FET [75, 76] have been reported. While the former was fabricated using regrowth of a GaN interlayer followed by MOCVD dielectric deposition on a trenched structure, the latter uses only n-type GaN layers with submicron fin-shaped channels.

9.7.2.2 4H-SiC Trench MISFETs

Although BV of 4H-SiC MISFETs was increased to 1.1 kV in 1997 [77] and 1.4 kV in 1998 [78] from that of the first 4H-SiC trench MISFET (i.e., 0.26

Authors and ref.	Otake et al. [68]	Kodama et al. [69]	Oka et al. [70]	Oka et al. [71]	Oka et al. [72]
Year	2008	2008	2014	2015	2016
Breakdown voltage (kV)	–	0.18	1.6	1.25	1.6
Specific on-resistance ($m\Omega cm^2$)	9.3	–	12.1	1.8	2.7

Authors and ref.	Gupta et al. [73]	Gupta et al. [74]	Sun et al. [75]	Zhang et al. [76]
Year	2017	2017	2017	2017
Breakdown voltage (kV)	0.99	1.4	0.8	1.2
Specific on-resistance ($m\Omega cm^2$)	2.6	2.2	0.36	0.2

Figure 9.21 Reported values of BV and $R_{on}A$ of GaN trench MISFETs on freestanding substrates [68–76].

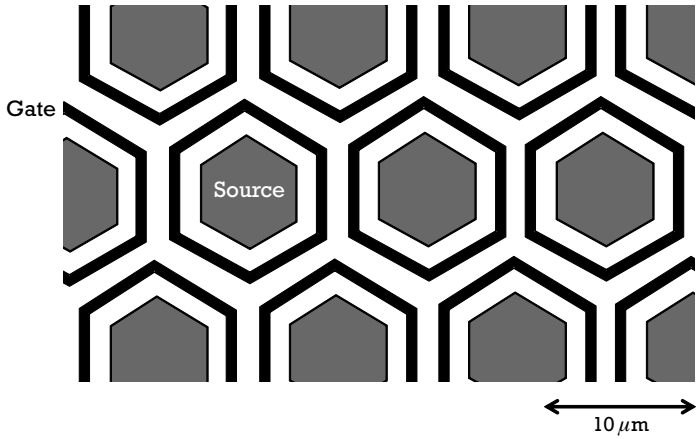

Figure 9.22 Schematic plan view of a regular hexagonal-trench gate layout [71, 72].

kV [67]), a very strong electric field developed across the gate insulator limited *BV* of 4H-SiC trench MISFETs.

Even in the case of silicon-trench MOSFETs, a strong electric field is developed in the gate oxide at the bottom corner of the silicon trench [79]; however, the electric field in the underlying semiconductor (E_S) is weak, 0.3 MV/cm [80]. On the other hand, E_s becomes high, namely, 3.75 MV/cm [81] for GaN and 2.50 MV/cm for 4H-SiC [82] (see Section 2.6). According to Gauss's law, the electric field in a gate insulator (E_I) is related to E_S as follows:

$$E_I = (\varepsilon_r/\varepsilon_I)E_S \tag{9.29}$$

where ε_r and ε_I are respectively relative permittivities of the semiconductor and the insulator. Since ε_r parallel to the *c*-axis is 10.4 for GaN [83] and 10.0 for 6H-SiC [84] (see Section 2.7) and ε_I is 7.5 for Si_3N_4 and 3.9 for SiO_2 [85], E_I becomes large, namely, 5.2 MV/cm in the case of Si_3N_4 on GaN [68], and 6.4 MV/cm in the case of SiO_2 on 4H-SiC [67]. These E_I values are close to dielectric strength (≈ 10 MV/cm for both Si_3N_4 and SiO_2 [85]), resulting in destruction of gate insulator at the trench bottom during application of high V_{DS} [67].

Shielding such high E_I is thus indispensable; however, to the author's knowledge, no GaN shielded-trench MISFETs have been reported. In contrast, in 2002, p^+ shielding regions, which are short-circuited to the source terminal, were first incorporated at the bottom of the trench of 4H-SiC trench MISFETs (Figure 9.23[a]) [86]. *BV* of such 4H-SiC shielded trench MISFETs increased to 3 kV for a 50-μm-thick drift layer doped at

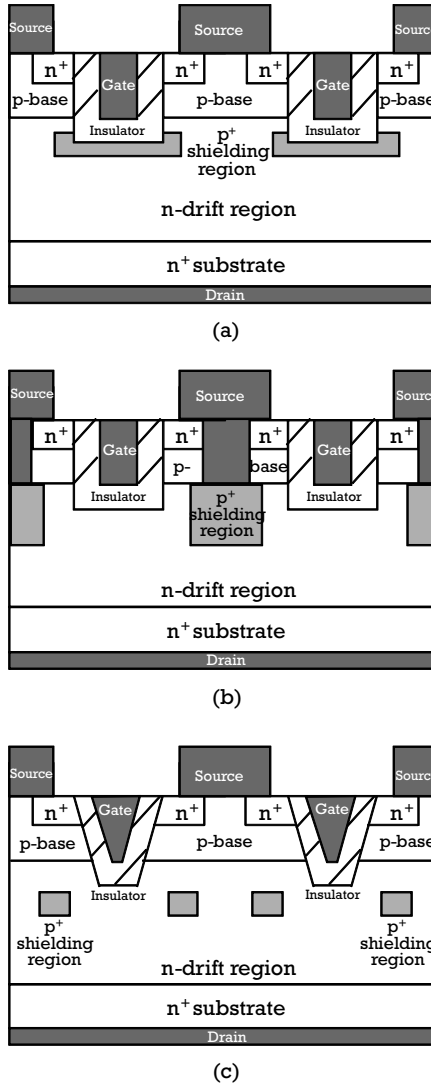

Figure 9.23 Schematic cross-sectional views of p^+ shielded (a) single-trench [79], (b) double-trench [88], and (c) V-groove trench MISFETs [90].

8.5×10^{14} cm^{-3} [86] and 5 kV for a 115-μm-thick drift layer doped at 7.5×10^{14} cm^{-3} [87]. However, reported $R_{on}A$ values of these 4H-SiC trench MISFETs were relatively large: 18 [67], 180 [77], 311 [78], 120 [86], and 228 $m\Omega cm^2$ [87].

In 2011, 4H-SiC MISFETs with source and gate trenches (so-called double trenches [Figure 9.23(b)]) were reported with very low $R_{on}A$: 0.79

mΩcm^2 for BV = 630V ($N_{drift} = 1.8 \times 10^{16}$ cm^{-3}; $t_{drift} = 5\,\mu$m) and 1.41 mΩcm^2 for BV = 1260V ($N_{drift} = 7.5 \times 10^{15}$ cm^{-3}; $t_{drift} = 8\,\mu$m) [88]. As described in Section 8.8, such a double-trench structure is also effective for reducing the electric field in trench SBDs. It has to be noted that t_{sub} was thinned down to 100 μm in [88]. Measured μ_{inv} on the trench sidewalls of the double-trench MISFETs was relatively small (i.e., 11 cm^2/Vs) [88]. According to Harada et al. [89], the deep p$^+$ regions create a JFET under the trench with a potential barrier that reduces the electric field at the bottom of the trenches, and E_I can be reduced to less than 3 MV/cm if the deep p$^+$ regions are formed 1.2 μm deeper than the bottom of the gate trench.

9.7.2.3 4H-SiC V-groove Trench MISFETs

A V-groove MISFET that utilizes the 4H-SiC $(0\bar{3}3\bar{8})$ face for the channel region is shown in Figure 9.23(c) [90]. Its fabrication process starts by growing a 12-μm-thick n-type drift layer doped at 4.5×10^{15} cm^{-3}. The p$^+$ shielding regions are then formed by aluminum-ion implantation, followed by growth of a 3-μm-thick n-type drift layer doped at 7×10^{15} cm^{-3}. To form a 0.6-μm-long channel on the trench sidewalls, p-base and n$^+$ source regions are implanted, respectively, with aluminum and phosphorus. BV and $R_{on}A$ were, respectively, 1,700V and 3.6 mΩcm^2, in contrast to 575V and 3.1 mΩcm^2 for a V-groove MISFET fabricated without the p$^+$ shielding regions. It was reported that μ_{inv} along the trench sidewalls was 80 cm^2/Vs [91] and that a design in which the p$^+$ regions occupy 30% of the active area balances BV and $R_{on}A$ [92].

9.7.3 SJ MISFETs

According to Gauss's Law, BV for a given SJ drift layer (Figure 9.17[c]) reaches a maximum when the sheet charge in each n-or p-type column Q_s is given as

$$Q_s = qN_D W_n = qN_A W_p = \varepsilon_r \varepsilon_o E_{critical} \tag{9.30}$$

where W_n and W_p are, respectively, widths of n- and p-type columns. $R_{drift}A$ is expressed as

$$R_{drift}A = \rho_{drift}\, t_{drift}(P/W_n) \tag{9.31}$$

where trench depth is approximated by t_{drift}. From (2.16),

$$\rho_{drift} = 1/(qN_D\mu_n) \tag{9.32}$$

putting (9.30) and (9.32) into (9.31) leads to the following expression:

$$R_{drift}A = t_{drift}P/(\mu_n Q_s) \tag{9.33}$$

If the electric field along the trench is assumed to be uniform,

$$t_{drift} = BV/E_{critical_SJ} \tag{9.34}$$

where $E_{critical_SJ}$ is critical electric field of an SJ drift layer. From (9.30), (9.33), and (9.34), it follows that

$$R_{drift}A = BV\,P/(\varepsilon_r\varepsilon_0\mu_n E_{critical_SJ}^2) \tag{9.35}$$

As derived in (2.22), $R_{drift}A$ of a conventional n-type drift layer is given as

$$R_{drift}A = 4BV^2/(\varepsilon_r\varepsilon_0\mu_n E_{critical_conv}^3) \tag{9.36}$$

where $E_{critical_conv}$ is the critical electric field of a conventional n-type drift layer. Comparing (9.35) with (9.36) clarifies the following advantages of an SJ drift layer:

- $R_{drift}A$ increases linearly with BV, which is opposed to the quadratic increase for a conventional n-type drift layer.
- $R_{drift}A$ decreases linearly with P because, according to (9.30), N_D and N_A must be increased with decreasing P. Larger N_D reduces ρ_{drift} (9.32) and hence $R_{drift}A$.

Note, however, that $E_{critical_SJ}$ becomes smaller than $E_{critical_conv}$ because a high electric field extends over a larger distance, thereby producing enhanced impact ionization [93].

To the author's knowledge, no GaN SJ MISFETs have been reported. The only 4H-SiC SJ MISFET reported to date is a V-groove MISFET with a drift layer formed by ion implantation [94]. The epitaxially grown n-type drift layer was 6.0-μm-thick and doped at 3×10^{15} cm^{-3}, and p-type columns with 3-μm-deep 3×10^{16}-cm^{-3} box profiles were formed with high-energy (up to 9 MeV) aluminum ion implantation. A 2-μm-thick epitaxial layer was then grown on the SJ structure, and the V-groove MISFET structure (Figure 9.23[c]) was fabricated. The resultant V_{th} of 3.4V was the same level as that of a conventional 4H-SiC V-groove MISFET. BV and $R_{on}A$ were, respectively, 820V and 0.97 mΩcm^2.

The impact of the SJ structure should appear more clearly in regard to higher-*BV* MISFETs. Moreover, fabrication of such SJ MISFETs will require trench-filling epitaxy (as described in Section 6.6).

9.8 Summary

This chapter starts by reviewing the physics of MIS capacitors and AlGaN/GaN heterostructures to provide an understanding of MISFET and HFET operations. Detailed analysis of $R_{on}A$ is carried out by taking a reported GaN MIS HFET and a 4H-SiC planar MISFET as examples. The chapter also introduces reported device performances of GaN MESFETs, GaN p^+-gate HFETs, GaN trench MISFETs, 4H-SiC trench MISFETs, and 4H-SiC V-groove MISFETs. Finally, with respect to SJ MISFETs, the chapter describes the concept of charge balance and introduces the very recently reported device performance of 4H-SiC V-groove SJ MISFETs.

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CHAPTER

10

Contents

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10.8 SiC IGBTs

10.9 Summary

Bipolar Power Diodes and Power-Switching Devices

10.1 Introduction

As stated in Section 8.1, a forward voltage-drop V_F (at forward current I_F [Figure 1.8]) of a unipolar power diode becomes less than V_F of a bipolar power diode as long as the voltage drop across the drift layer is negligible. In other words, V_F of a bipolar power diode becomes smaller than V_F of a unipolar power diode when the voltage rating is high. With regards to power dissipation of 4H-SiC power diodes, it was theoretically derived that a bipolar power diode is preferred when reverse voltage exceeds 2 kV and operating frequency is below 30 kHz [1]. With respect to GaN bipolar power diodes, on the other hand, that voltage and frequency should decrease on the basis of the measured stored charge of a 1.6-kV GaN bipolar power diode being only 5.6% of that of a Si bipolar power diode [2]. This stored-charge difference

is due to the shorter carrier lifetime of GaN; however, effective carrier lifetime (under high-level injection) of GaN is increased by photon recycling (see Chapter 4), which led to a demonstration of a GaN bipolar power diode with very high breakdown voltage *BV* (i.e., 5.0 kV) [3]. Bipolar power diodes include p-n diodes (Figure 10.1[a]) and p-i-n diodes (Figure 10.1[b]). In addition, p-n-p-n diodes, called Shockley diodes, (Figure 10.1[c]) have been developed, although they are functionally two-terminal power-switching devices. All these diodes adopt a non-self-aligned mesa-type configuration, as explained in Section 3.7.

With respect to power-switching devices, GaN bipolar ones have not been reported. Although GaN/InGaN heterojunction bipolar transistors

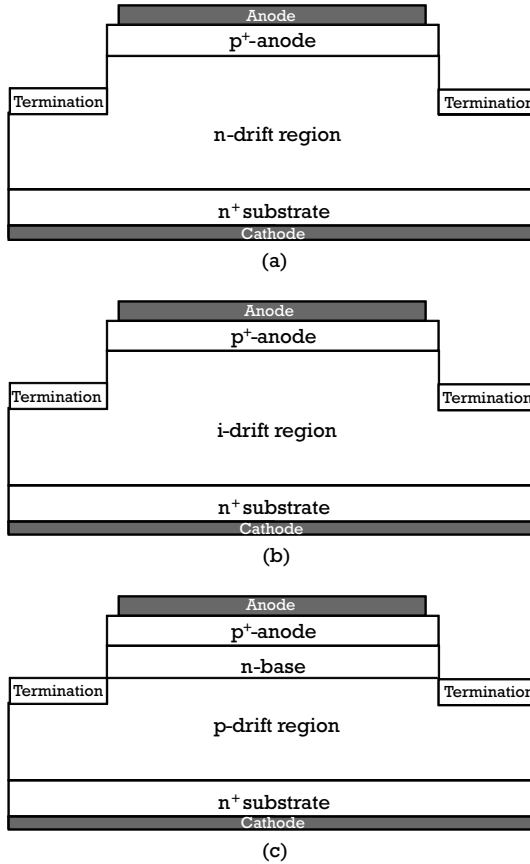

Figure 10.1 Schematic cross-sectional views of bipolar power diodes: (a) p-n diode, (b) p-i-n diode, and (c) Shockley diode (i.e., p-n-p-n diode). Although "i" stands for intrinsic, a lightly-doped n-type layer is usually used for an i-drift layer in the case of a wide-bandgap semiconductor p-i-n diode.

were fabricated on freestanding GaN substrates [4], the transistors were designed for rf small-signal amplification. However, on the basis of a bipolar junction transistor (BJT) being the first bipolar power-switching device based on silicon, this chapter briefly introduces the possible performance of a n-p-n GaN BJT as a candidate for the first GaN bipolar power-switching device.

As essential components of 4H-SiC power-switching devices, BJTs (Figure 10.2[a]), thyristors (Figure 10.2[b]), and insulated-gate bipolar transistors (IGBTs) (Figure 10.2[c]) have been fabricated. 4H-SiC n-p-n BJTs with breakdown voltage up to 1.7 kV are commercially available, and their characteristics have been modeled and simulated [5]. Thyristors are

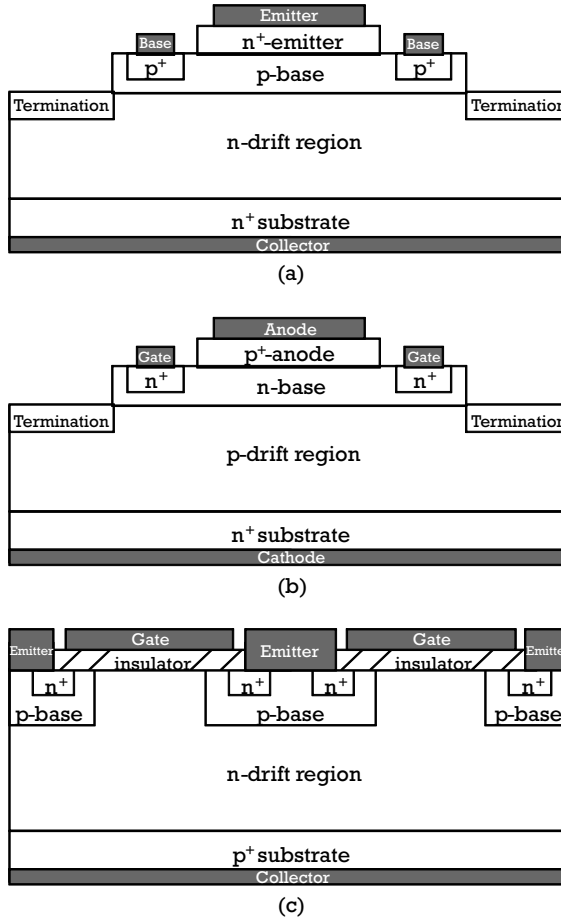

Figure 10.2 Schematic cross-sectional views of bipolar power-switching devices: (a) BJT, (b) thyristor, and (c) IGBT.

formed by incorporating gate electrodes in Shockley diodes (Figure 10.1[c]) so that they can be switched on for valuable lengths of time during on-state. A conventional thyristor is usually turned off by lowering the anode current below a holding current, I_h. However, gate-turn-off thyristors (GTOs) and emitter-turn-off thyristors (ETOs) can be turned off, respectively, with negative gate and emitter currents; for example, up to 22-kV 4H-SiC GTOs [6] and 22-kV 4H-SiC ETOs [7] have been demonstrated. In BJTs and thyristors, control electrodes (i.e., base electrodes in the case of BJTs and gate electrodes in the case of thyristors) make ohmic contacts with semiconductor regions. In contrast, an insulated-gate structure is used in IGBTs. The name IGBT is derived from its operation based on the insulated-gate field-effect transistor and the bipolar transistor. The structure of an n-channel IGBT (Figure 10.2[c]) is similar to that of an n-channel MISFET (Figure 9.17[a]), except that an n^+ substrate in the MISFET is replaced with a p^+ substrate in the IGBT. Although the backside electrode of IGBTs is conventionally called a collector electrode, it functions as an emitter electrode of a p-n-p BJT (Figure 10.3). Up to 27-kV 4H-SiC n-channel IGBTs have been reported [8].

This chapter covers only planar types of the above-described bipolar power diodes and power-switching devices. Note, however, that similar to the MISFETs described in Section 9.6, trench and V-groove structures have also been applied to IGBTs [9–11].

10.2 Optimum Design of a One-Dimensional p-n Diode

Section 3.5 considers depletion-region width, W_{Dn}, of a reverse-biased one-dimensional p^+n diode when drift-layer thickness W_n is equal to or larger than W_{Dn}, which is given by (3.31), by replacing Ψ_{bi}–V with V_R

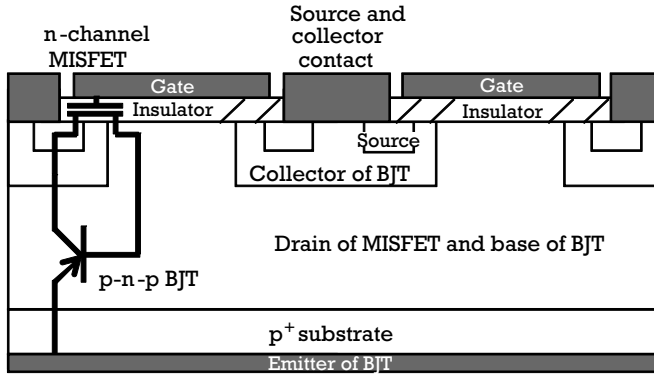

Figure 10.3 Schematic cross-section of an n-channel IGBT viewed as a combination of an n-channel MISFET and a p-n-p BJT.

$$W_{Dn} \approx (2\varepsilon_r\varepsilon_o V_R/qN_D)^{0.5} \tag{10.1}$$

where ε_r is relative permittivity parallel to the *c*-axis, ε_o is permittivity in a vacuum, V_R is reverse bias, and N_D is net donor density in a uniformly doped drift layer. When $W_n = W_{Dn}$ at a rated voltage (Figure 10.4) and $W_{Dn} >> W_{Dp}$, BV is given as

$$BV \approx E_{max}W_n/2 \tag{10.2}$$

Putting ε_r of 10.4 for GaN [12] and 10.0 for 4H-SiC [13] (see Section 2.7) and the highest critical electric field ($E_{critical}$) ever reported (i.e., 3.75 MV/cm [14] for GaN and 2.50 MV/cm for 4H-SiC [15]) (see Section 2.6), respectively, into (10.1) and (10.2) leads to an optimum design of a one-dimensional p-n diode with a uniformly doped drift layer (as shown in Figure 10.5).

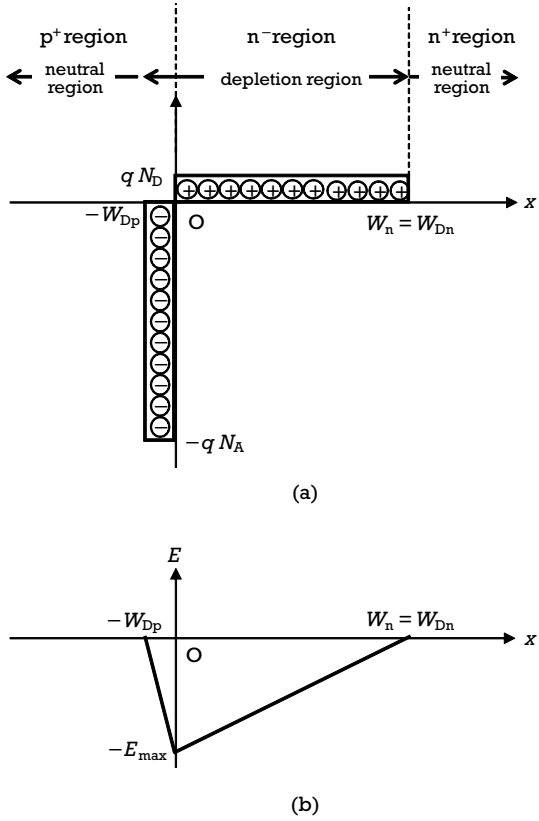

Figure 10.4 Reverse-biased abrupt $p^+/n^-/n^+$ junction in which depletion-region width is equal to drift-layer thickness: (a) space-charge distribution under depletion approximation and (b) electric-field distribution.

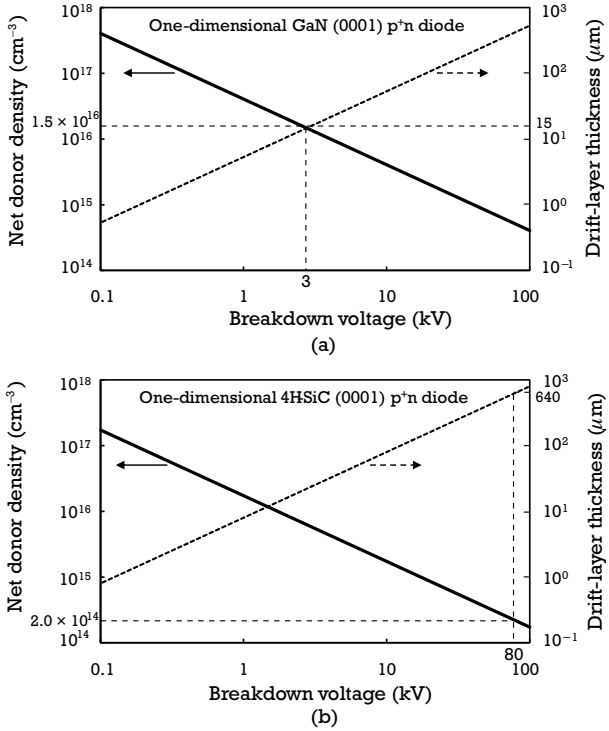

Figure 10.5 Optimum design of (a) GaN (0001) and (b) 4H-SiC (0001) abrupt $p^+/n^-/n^+$ junction in which depletion-region width is equal to drift-layer thickness.

As source gasses for MOCVD of n-type GaN, TMG, ammonia (NH_3), and silane (SiH_4) are most frequently used (see Section 6.2). Residual carbon background is known to be minimized by performing MOCVD under a large partial pressure of NH_3. For instance, it was found that a NH_3/TMG flow-rate ratio exceeding 1,000 decreases concentration of unintended carbon acceptors (i.e., about 5×10^{16} cm^{-3}) in epitaxially grown GaN (0001) to $1 - 2 \times 10^{16}$ cm^{-3} [16] (open symbols in Figure 10.6). If minimum controllable N_D is assumed to be 1.5×10^{16} cm^{-3}, the highest BV is predicted from Figure 10.5(a) to be about 3 kV when W_n is 15 μm. These values are close to the experimentally measured ones: BV = 3.7 kV in the case of $N_D = 6 \times 10^{15}$ cm^{-3} and W_n = 40 μm [16] and BV = 1.1 kV in the case of $N_D = 2 \times 10^{16}$ cm^{-3} and W_n = 10 μm [17]. To achieve higher BV, a nonuniformly n-type-doped drift layer, which is described in Section 10.3, has been employed [3, 18, 19].

In the case of CVD of 4H-SiC, on the other hand, minimum controllable N_D can be greatly decreased by increasing the carbon-to-silicon input-gas ratio (C/Si ratio); for example, it can be decreased from 1×10^{16} cm^{-3}

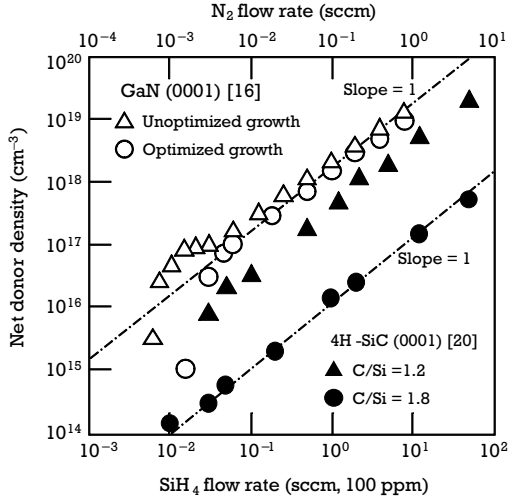

Figure 10.6 Reported net donor density in epitaxially grown GaN (0001) and 4H-SiC (0001) as functions of flow rates of SiH_4 and N_2, respectively [16, 20].

to 2×10^{14} cm^{-3} by increasing the C/Si ratio from 1.2 to 1.8 [20] (solid symbols in Figure 10.6). From Figures 10.5(b) and 10.6, it is predicted that the highest BV is about 80 kV when drift-layer thickness is 640 μm. Using such a thick drift layer, however, greatly increases $R_{on}A$. By making W_n smaller than W_{Dn} (to form a so-called p-i-n junction as shown in Figure 10.7[a]), the electric-field profile becomes trapezoidal, as shown by the solid lines in Figure 10.7(b). As the doping level in the drift layer (N_{D1}) decreases, the electric-field profile approaches a rectangle, as shown by the dashed lines in Figure 10.7(b). BV thus approaches the maximum, given as

$$BV_{max} = E_{max} W_n \tag{10.3}$$

To take advantage of the lower and controllable N_D, 4H-SiC bipolar diodes often use a p-i-n junction, which is described in Section 10.4. Note that although "i" stands for intrinsic, a lightly-doped n-type layer is usually used as an i-drift layer.

10.3 GaN p-n Diodes with a Nonuniformly Doped Drift Layer

To reduce the peak electric field at the p-n junction, a GaN p-n diode with double drift layers consisting of a 5-μm-thick n-type GaN layer doped at 1×10^{15} cm^{-3} and a 15-μm-thick n-type GaN layer doped at 1×10^{16} cm^{-3} was fabricated; the resultant BV was over 3 kV [18]. Triple drift layers were also applied to GaN p-n diodes with the following properties: BV = 3.48 kV

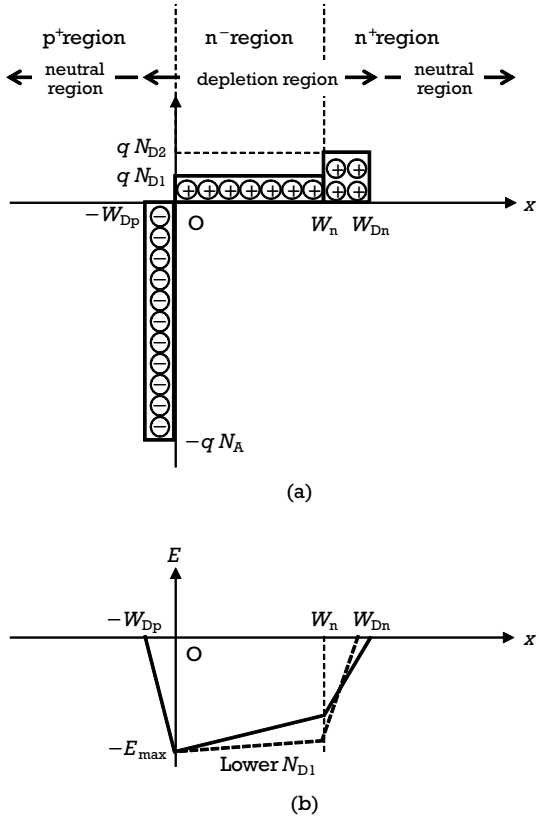

Figure 10.7 Reverse-biased abrupt $p^+/n^-/n^+$ junction: (a) space-charge distribution under depletion approximation and (b) electric-field distribution. Compared to the solid lines in (b), the dashed lines in (b) represent the electric-field distribution in the case of lower N_{D1}.

for a 6-μm-thick GaN layer doped at about 1×10^{15} cm^{-3}, a 11-μm-thick n-type GaN layer doped at 3×10^{15} cm^{-3}, and a 15-μm-thick n-type GaN layer doped at 1.2×10^{16} cm^{-3} [19] and BV = 5.0 kV for a 5.5-μm-thick undoped GaN with a residual silicon concentration of $< 2 \times 10^{15}$ cm^{-3}, a 22-μm-thick n-type GaN with a silicon concentration of 9×10^{15} cm^{-3}, and a 5.5-μm-thick n-type GaN with a silicon concentration of 1.6×10^{16} cm^{-3} [3].

Owing to extrinsic photon recycling (EPR)—see Section 4.6—differential specific on-resistance $R_{on}A^{diff}$ (see Section 1.3.2) of reported GaN p-n diodes [3, 17–19] is comparable to that of 4H-SiC p-i-n diodes [21, 22] (Figure 10.8). Due to a typical limit on power dissipation of a semiconductor package (300 Wcm/^{2} [23]), however, EPR does not practically work in the case of GaN p-n diodes. As shown as an example in Figure 10.9, the

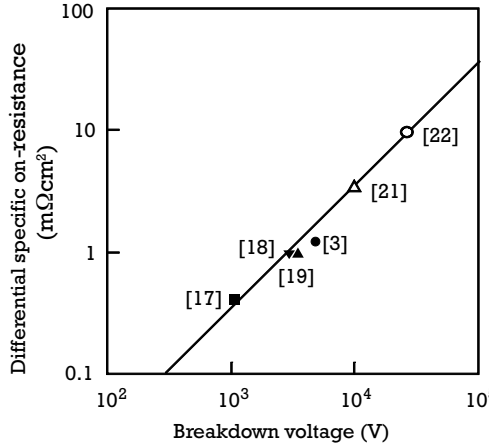

Figure 10.8 Reported differential specific on-resistance of GaN p-n diodes (solid symbols [3, 17–19]) and 4H-SiC p-i-n diodes (open symbols [21, 22]) versus breakdown voltage.

maximum allowable current density of a GaN 5.0 kV p-n diode [3] is 90 A/cm^2, and its corresponding forward voltage is 3.4V. The latter voltage, however, is comparable to that of a 4H-SiC 3.5-kV junction-barrier Schottky diode (see Section 8.9) (i.e., 3.1V) [24]. In contrast, EPR should work effectively in the case of a zero-offset (see Figure 1.7[a]) GaN n-p-n BJT, which is described in Section 10.5.4.

10.4 4H-SiC p-i-n Diodes

10.4.1 Reported Results Concerning 4H-SiC p-i-n Diodes

An epitaxially grown anode was used in a 4H-SiC p-i-n diode to achieve BV of 6.2 kV [25]. In the case of ion-implanted anodes, the forward characteristics were reported to be sensitive to junction depth and activation process [26]. A 4H-SiC p-i-n diode with a 100-μm-thick drift layer doped at $1 - 3 \times 10^{14}$ cm^{-3} reportedly demonstrated V_F = 7.1V at 100 A/cm^2 and BV of 8.6 kV [27]. Co-implantation of aluminum, carbon, and boron was also used to form an anode of a 4H-SiC p-i-n diode with a 40-μm-thick drift layer doped at 1×10^{15} cm^{-3} [28]; V_F at 100 A/cm^2 and BV were reported as 4.7V and about 4.5 kV, respectively. These V_F values are not sufficient in terms of the limit on the power dissipation of a semiconductor package (as shown in Figure 10.9).

Since conductivity modulation (see Section 3.7) has not been fully achieved by using aluminum-ion implantation [29], carrier lifetime has been improved by epitaxial growth [30] and elimination of carbon-vacancy defects

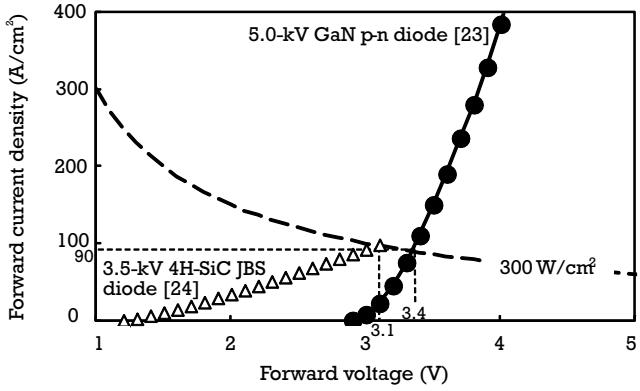

Figure 10.9 Reported current/voltage characteristics of a 5.0-kV GaN p-n diode [3] and a 3.5-kV 4H-SiC junction barrier Schottky diode [24], together with a curve showing the power-dissipation limit of a semiconductor package (i.e., 300 W/cm^2) [23].

(i.e., carbon-ion implantation [31] and thermal oxidation [32]). Due to improved crystal growth (i.e., reduced micropipe and defect densities) and epitaxy (i.e., reduced epitaxial defects), carrier lifetime of epitaxial 4H-SiC was improved and a 10-kV p-i-n diode with V_F of 3.9V at 100 A/cm^2 was demonstrated in 2004 [30]. The i-drift layer used was 100-μm-thick and doped at 2×10^{14} cm^{-3}. By applying carbon-ion implantation or thermal-oxidation, a 4H-SiC p-i-n diode with V_F of about 4.0V at 100 A/cm^2 was demonstrated in 2012 [33]. Its BV was calculated to be 18.5 kV in the case of a 120-μm-thick i-drift layer doped at 7×10^{13} cm^{-3}. $R_{on}A^{diff}$ was 3.3 mΩcm^2 at BV of 12.9 kV (for a 100-μm-thick drift layer doped at 3×10^{14} cm^{-3}) [21] and 9.72 mΩcm^2 at BV of 26.9 kV (for a 268-μm-thick drift layer doped at $1 - 2 \times 10^{14}$ cm^{-3}) [22], as shown by the open symbols in Figure 10.8.

10.4.2 Stored Charge in Forward-Biased 4H-SiC p-i-n Diodes

Under high-level injection (see Section 3.6.2), forward-current density is given as

$$J_F = J_S^{HL} \exp(qV/2kT) \tag{10.4a}$$

$$J_S^{HL} = \{2qD_aN_C^{0.5}N_V^{0.5} \tanh(d/L_a)/L_a/[1-0.25\tanh^4(W_n/2L_a])^{0.5}\} \times \exp[-(E_g+qV_M)/(2kT])] \tag{10.4b}$$

where V_M is the voltage drop across an i-drift layer, and D_a is ambipolar diffusivity defined as

$$D_a = 2D_nD_p/(D_n + D_p) \tag{10.4c}$$

where D_n and D_p are, respectively, electron and hole diffusivities, and L_a is ambipolar diffusion length defined as

$$L_a = (D_a \tau_{HL})^{0.5} \tag{10.4d}$$

where τ_{HL} is high-level injection lifetime. Average carrier density and stored charge in the i-drift layer are thus given as

$$n_{ave} = J_F \tau_{HL}/qW_n \tag{10.5}$$

and

$$Q_s = qW_n n_{ave} = J_F \tau_{HL}. \tag{10.6}$$

According to (10.6), Q_s increases with τ_{HL} at fixed J_F. Therefore, decreasing τ_{HL} is necessary for reducing Q_s, although large τ_{HL} is needed for reducing V_F (see Section 10.4.1).

To estimate Q_s, the reported forward current-density/voltage characteristics of a 26.9-kV 4H-SiC p-i-n diode [22] are taken as an example in the following. When the limit on the power dissipation of a semiconductor package is 300 W/cm^2 [23], J_F should be less than 70 A/cm^2 (Figure 10.10). If τ_{HL} in (10.6) is taken as 3 μs [22], maximum Q_s is estimated to be 2.1×10^{-4} C/cm^2.

10.4.3 Reverse Recovery of 4H-SiC p-i-n Diodes

As described in Section 1.2, a power diode is used as a reverse conducting device in the case of an inductive load (e.g., a motor). When the diode is a p-i-n diode, power dissipation from the on-state to the off-state is larger than that from the off-state to the on-state. This is because the charges in the i-drift layer stored during the on-state are removed first. The phenomenon by which a large reverse current is produced before the p-i-n diode can support high voltage is called "reverse recovery."

As illustrated in Figure 10.11, anode current density decreases from J_F at a rate $-k$ until W_{Dn} becomes W_n. Just after the current density reaches a minimum (i.e., $J_R = -k\, t_{rr}$), voltage rises rapidly to the supply voltage [34]. The charge removed during reverse recovery is given as

$$Q_{rr} = J_R t_{rr}/2 \tag{10.7}$$

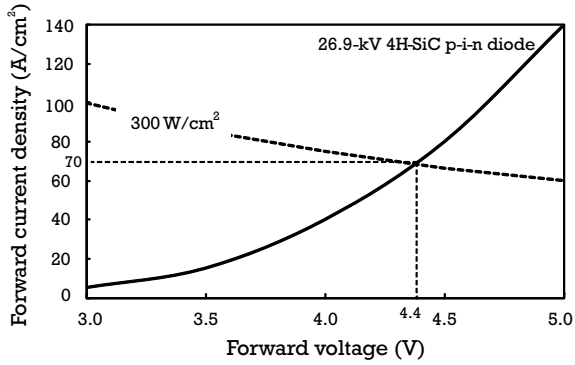

Figure 10.10 Reported current/voltage characteristics of a 26.9-kV 4H-SiC p-i-n diode [22], together with a curve showing the power dissipation-limit of a semiconductor package (i.e., 300 W/cm^2) [23].

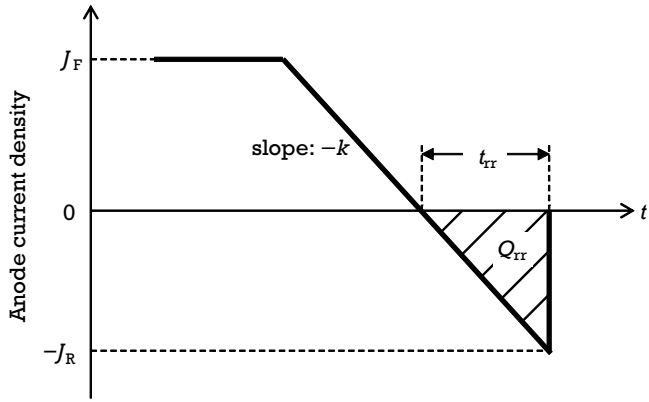

Figure 10.11 Schematic anode current-density and voltage waveforms of a p-i-n diode during reverse recovery.

where t_{rr} is the reverse-recovery time shown in Figure 10.11. From (10.6) and (10.7), t_{rr} and J_R are expressed as

$$t_{rr} = (2\,\tau_{HL}\,J_F/k)^{0.5} \tag{10.8}$$

and

$$J_R = (2\,k\,\tau_{HL}\,J_F)^{0.5}. \tag{10.9}$$

For example, when τ_{HL} = 3 μs [22], J_F = 70 A/cm^2, and $k = 2 \times 10^7$ A/cm^2/s, t_{rr} and J_R are calculated to be 4.6 μs and 92 A/cm^2, respectively.

10.5 n-p-n BJTs

The first SiC BJT, comprising an n-type emitter layer doped at 10^{20} cm^{-3}, a 0.8-μm-thick p-type base layer doped at 4×10^{17} cm^{-3}, and an n-type collector layer doped at 5×10^{18} cm^{-3}, was reported in 1977 [35]; however, due to heavy collector doping, its open-base collector-to-emitter breakdown voltage BV_{CEO} was quite low (i.e., 50V). In consideration of that drawback, this section first describes the designs of collector and base layers. Subsequently, the section examines the critical collector-current density for "second breakdown," which is characterized as an abrupt reduction in the voltage drop across a BJT. Next, the section discusses the expected performance of GaN BJTs and the reported performance of 4H-SiC BJTs.

10.5.1 Collector-Layer Design

This section neglects the influence of conductivity modulation. Open-emitter collector-to-base breakdown voltage BV_{CBO} is the same as the BV of a p-i-n diode (see Section 10.2), namely,

$$BV_{CBO} = E_{critical} W_N - q N_{D1} W_N^2 / (2\varepsilon_r \varepsilon_o) \tag{10.10}$$

Specific drift-region resistance $R_{drift}A$ is given as

$$R_{drift}A = W_N / (q \mu_n N_{D1}) \tag{10.11}$$

where μ_n is electron mobility. Eliminating N_{D1} from (10.10) and (10.11) gives the following equation:

$$R_{drift}A = W_N^3 / [2\mu_n \varepsilon_r \varepsilon_o (E_{critical} W_N - BV_{CBO})] \tag{10.12}$$

Differentiating (10.12) with respect to x (shown in Figure 10.7) gives

$$dR_{drift}A/dx = W_N^2 (2E_{critical} W_N - 3BV_{CBO}) / [2\mu_n \varepsilon_r \varepsilon_o (E_{critical} W_N - BV_{CBO})^2] \tag{10.13}$$

$R_{drift}A$ reaches minimum when $dR_{drift}A/dx = 0$, namely,

$$W_{N_optimum} = (3/2)(BV_{CBO}/E_{critical}) \tag{10.14a}$$

and

$$N_{D1_optimum} = (4/9)(\varepsilon_r \varepsilon_o E_{critical}{}^2/qBV_{CBO}). \quad (10.14b)$$

BV_{CEO} is related to BV_{CBO} by

$$BV_{CEO} = BV_{CBO}(1+\beta_0)^{-1/n} \quad (10.15)$$

where β_0 is common-emitter current gain at low current, and n is about 10 for SiC [36]. As shown in Figure 10.12, BV_{CEO}/BV_{CBO} is calculated to be larger than 0.5 as long as β_0 is less than 10^3. Here, $BV_{CBO} = 2BV_{CEO}$ is thus assumed. Equations (10.14a) and (10.14b) are respectively expressed as

$$W_{N_optimum} = 3BV_{CEO}/E_{critical} \quad (10.16a)$$

and

$$N_{D1_optimum} = (2/9)(\varepsilon_r \varepsilon_o E_{critical}{}^2/qBV_{CEO}) \quad (10.16b)$$

and shown in Figure 10.13.

10.5.2 Base-Layer Design

Charge density in the optimum collector layer is determined from (10.16a) and (10.16b) as

$$Q_{collector} = (2/3)(\varepsilon_r \varepsilon_o E_{critical}/q) \quad (10.17)$$

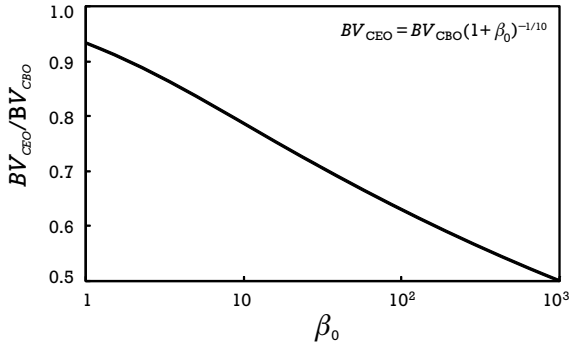

Figure 10.12 Ratio of BV_{CEO} to BV_{CBO} calculated using (10.15) as a function of common-emitter current gain at low current. n is assumed to be 10 [36].

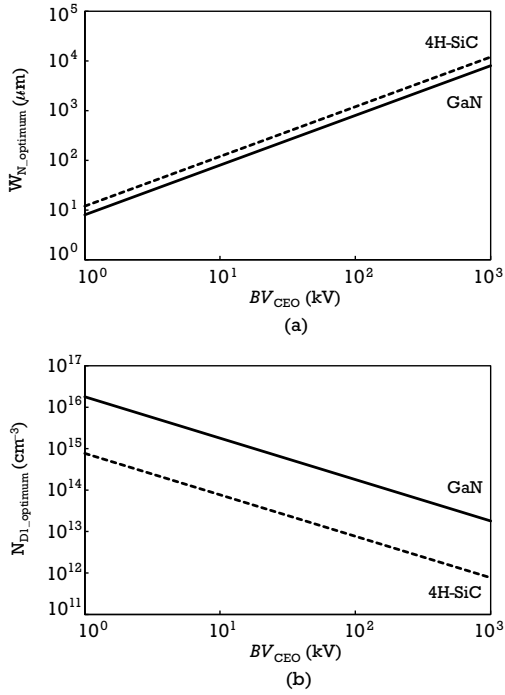

Figure 10.13 (a) $W_{N_optimum}$ and (b) $N_{D1_optimum}$ calculated from (10.16a) and (10.16b) as a function of BV_{CEO} in the case $BV_{CEO} = 2BV_{CBO}$.

which is 1.4×10^{13} cm^{-2} in the case of GaN and 9.2×10^{12} cm^{-2} in the case of 4H-SiC. Charge density in a base layer should be larger than $Q_{collector}$ to prevent emitter-collector punch through. In addition, base-layer thickness W_B should be less than electron diffusion length L_n (see Section 3.6.1.1) to achieve high β_0.

Moreover, a high base-doping level is desirable from the view point of reducing emitter-current crowding, which is caused by base-current-induced voltage drop in the p-type base layer [37]. However, the base-doping level should be low enough to maintain emitter-injection efficiency γ_E, which is a measure of emitter current produced by electron injection from the emitter into the base, and is expressed as [37]

$$\gamma_E = D_{nB} t_E N_{DE}^{+} / (D_{nB} t_E N_{DE}^{+} + D_{pE} W_B N_{AB}^{-}) \tag{10.18}$$

where D_{nB} and D_{pE} are, respectively, diffusivities for electrons in the base and holes in the emitter, N_{DE}^{+} and N_{AB}^{-} are, respectively, concentrations of ion-

ized donors in the emitter and acceptors in the base, and t_E is emitter-layer thickness.

10.5.3 Critical Collector-Current Density for Second Breakdown

In the case of silicon BJTs, a phenomenon called second breakdown is known to limit the safe operating area (namely, the voltage and current conditions over which the device can operate) [38]. Critical collector-current density J_{CSB} for second breakdown is expressed as [38]

$$J_{CSB} = \varepsilon_r \varepsilon_o v_s E_{critical}^2 / (2BV_{CBO}) \tag{10.19}$$

where v_s is electron saturation velocity (1×10^7 cm/s for Si [39]; 2.5×10^7 cm/s for GaN [40]; 3.3×10^6 cm/s for 4H-SiC [41]). When BV_{CBO} = 1.2 kV (i.e., $BV_{CEO} \approx 0.6$ kV), J_{CSB} is calculated to be 0.17 kA/cm^2 for silicon BJTs, 120 kA/cm^2 for GaN BJTs, and 15 kA/cm^2 for 4H-SiC BJTs. In the case of silicon BJTs, J_{CSB} lower than operational current-density is the cause for the second breakdown. In the cases of GaN and 4H-SiC BJTs, on the other hand, J_{CSB} is larger than operational current-density, suggesting that GaN and 4H-SiC BJTs are free from second breakdown.

10.5.4 GaN BJTs

Zero-offset current/voltage characteristics of a GaN n-p-n BJT were demonstrated, although the device had a quasi-vertical configuration formed on a sapphire substrate [42]. In the case of such zero-offset BJTs, EPR is expected to work effectively. As described in Section 4.6, the lateral extension of EPR in p-type GaN was determined to be about 10 μm from the edge of the p-type electrode. Therefore, GaN BJTs with 20-μm-spaced base fingers are considered to be the most area-efficient in terms of $R_{on}A$. Under the assumption of effective acceptor level E_A^{eff} determined in Section 4.6, current/voltage characteristics of 0.6-kV-class GaN BJTs (BV_{CBO} = 1.2 kV) with a non-self-aligned base mesa structure were simulated [43]. $R_{on}A$ of GaN BJTs can be lower that of state-of-the-art 0.6-kV-class 4H-SiC trench MISFETs [44]. However, the BJT structure that minimizes base current density remains to be optimized.

10.5.5 SiC BJTs

The first SiC BJTs (reported in 2001) demonstrated BV_{CEO} of 1.8 kV and β_0 of 20 [45]. β_0 was then increased to 50 for 2.7-kV BJTs [46], 63 for 21-kV BJTs [47], 73 for 0.6-kV BJTs [48], 110 for 0.27-kV BJTs [49], and 134 for

0.95-kV BJTs [50]. In 2011, β_0 of 257 and 335 were, respectively, attained for BJTs formed on 4H-SiC (0001) and $(000\overline{1})$ substrates, although BV_{CEO} of these BJTs were not reported [51]. These extremely large β_0 values were achieved by utilizing optimized device geometry and continuous epitaxial growth of the emitter-base junction, in combination with a deep-level-reduction process to improve the lifetime in the base layer.

10.6 Shockley Diodes

Since neither GaN nor 4H-SiC Shockley diodes have been reported, basic characteristics of a silicon Shockley diode, which form the basis for understanding thyristor characteristics, are reviewed hereafter. The basic structure of a one-dimensional Shockley diode is schematically shown in Figure 10.14. It consists of three p-n junctions: J1, J2, and J3. The width of the region doped at P_2 (W_{P2}) is much larger than the width of the other three regions, and P_2 is much lower than the other three doping levels.

10.6.1 Reverse Blocking of Shockley Diodes

In reverse-blocking mode, J1 and J3 are reverse-biased, while J2 is forward-biased. And most of the applied reverse bias is supported by the p_2-region. In the case that depletion-region width at breakdown is less than W_{p2}, avalanche multiplication causes breakdown at BV_R (Figure 10.15); in the opposite case, punch-through (namely, J2 being shorted to J3) causes breakdown at BV_R.

10.6.2 Forward Blocking of Shockley Diodes

In forward-blocking mode, J1 and J3 are forward-biased, while J2 is reverse-biased. Most of the applied anode voltage is thus supported by J2. When the anode voltage reaches BV_F (Figure 10.15), electron-hole pairs are generated (see Section 2.6) ([1] in Figure 10.16[a]). The generated electrons and holes are injected into the n_1- and p_2-neutral regions, respectively ([2] and [2′]

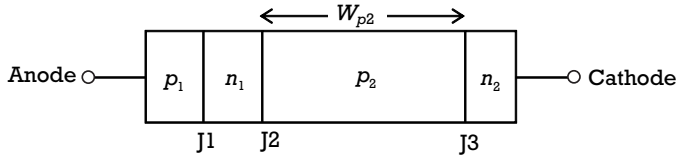

Figure 10.14 Schematic structure of a one-dimensional Shockley diode. In a typical silicon Shockley diode, net doping levels are $p_1 \approx 10^{20}$ cm^{-3}, $n_1 \approx 10^{18}$ cm^{-3}, $p_2 \approx 10^{14}$ cm^{-3}, and $n_2 \approx 10^{19}$ cm^{-3}.

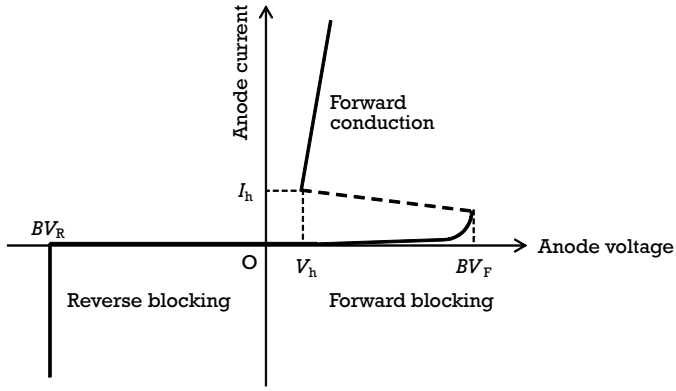

Figure 10.15 Schematic current/voltage characteristics of a Shockley diode.

in Figure 10.16[a]), resulting in a decrease of n_1- and p_2-depletion-region widths ([3] and [3′] in Figure 10.16[b]). To maintain charge neutrality, p_1- and n_2-depletion-region widths are also decreased ([4] and [4′] in Figure 10.16[b]), which leads to increased forward bias at J1 and J3 ([5] and [5′] in Figure 10.16[b]). This increased forward bias increases hole injection from the p_1-neutral region to the n_1-neutral region ([6] in Figure 10.16[b]) and electron injection from the n_2-neutral region to the p_2-neutral region ([6′] in Figure 10.16[b]), which further increases electron and hole injection into the p_1- and n_2-neutral regions ([2] and [2′] in Figure 10.16[a]). Such positive feedback reduces anode voltage from BV_F to V_h (Figure 10.15) and leads to forward conduction.

10.7 SiC Thyristors

SiC thyristors (Figure 10.2[b]) are formed by connecting gate electrodes to the n_1 region of Shockley diodes (Figure 10.17). As shown in Figure 10.18, thyristors can be turned on even when the anode voltage is less than BV_F (shown in Figure 10.15) by injecting electrons from the gate electrode. A 22-kV 4H-SiC GTO reported in 2014 used a 160-μm-thick p-type drift layer doped at 2×10^{14} cm^{-3} and demonstrated V_F of 5V at 25 A/cm^2 [6]. Due to the success of high-voltage SiC IGBTs described in Section 10.8, however, SiC thyristors are not so actively being developed right now.

10.8 SiC IGBTs

Since a 4H-SiC n-channel IGBT capable of attaining 13-kV blocking voltage was reported in 2007 [52], 10-kV [53], 12.5-kV [54], 16-kV [55], 22-kV

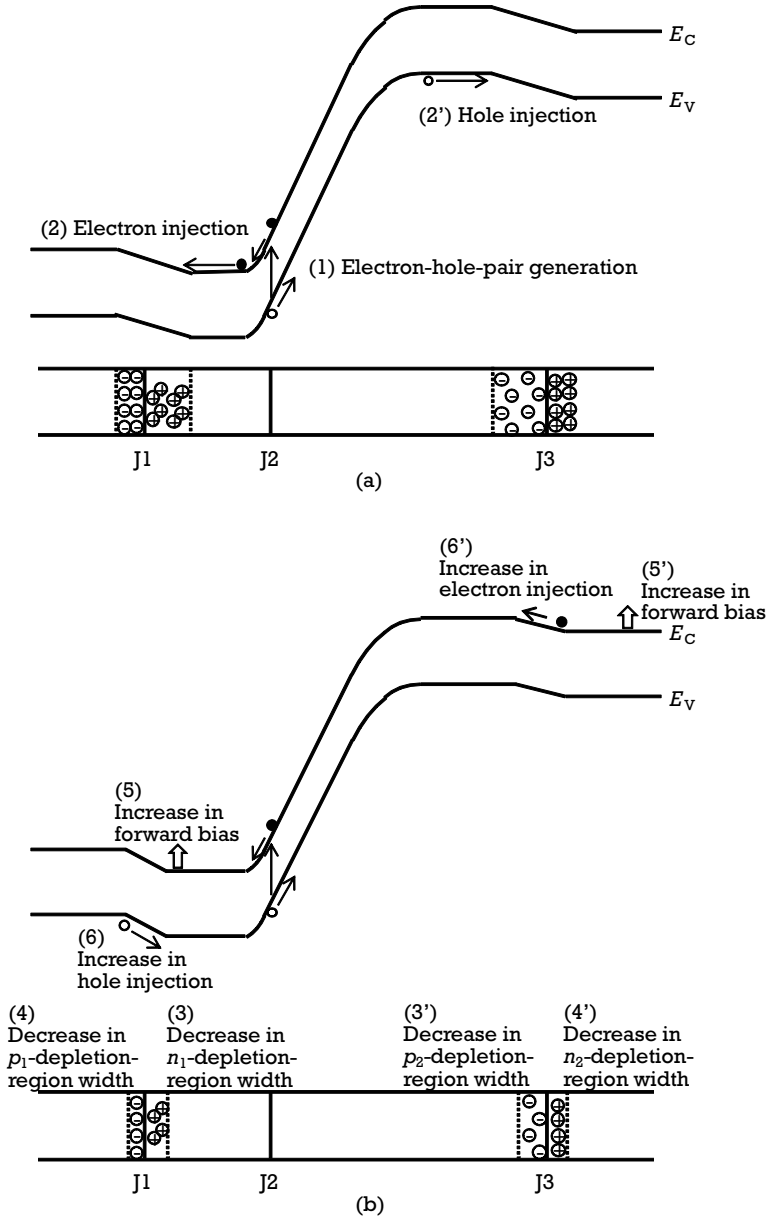

Figure 10.16 Schematic band diagrams illustrating the conditions immediately (a) before and (b) after anode voltage reaching BV_F shown in Figure 10.15.

[56], and 27-kV [8] n-channel IGBTs have been demonstrated. Owing to conductivity modulation (see Section 3.7), $R_{drift}A$ of IGBTs is greatly reduced from that of MISFETs (see Section 9.7). In contrast, the switching loss of

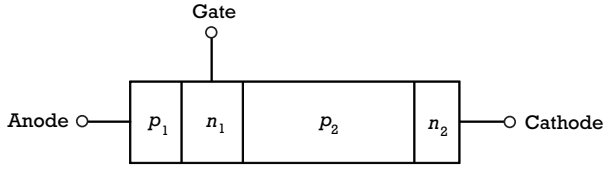

Figure 10.17 Schematic structure of a one-dimensional thyristor.

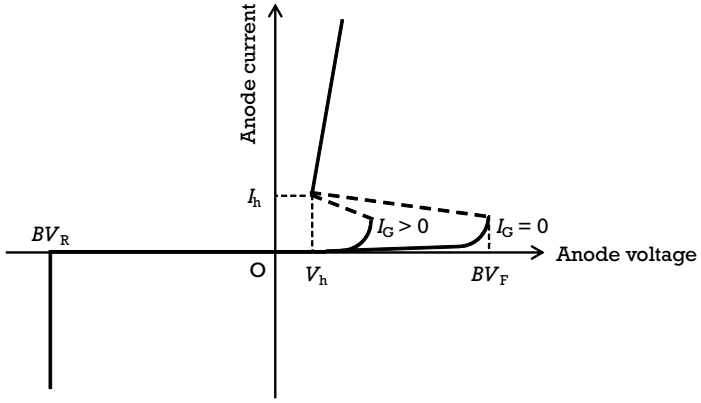

Figure 10.18 Schematic current/voltage characteristics of thyristor.

IGBTs is much larger than that of MISFETs. The reason for that switching-loss difference is similar to the reverse recovery of p-i-n diodes described in Section 10.4.3. Since the basic operating principles of SiC IGBTs are described in detail in elsewhere [57, 58], this section only provides a brief description of the turn-off characteristics of 4H-SiC IGBTs.

To turn IGBTs off, gate bias has to be reduced to zero (Figure 10.19[a]). When gate bias becomes lower than threshold voltage, electron current in the channel ceases. However, in the case of an inductive load, collector current is sustained by holes stored in the n-type drift region, as shown in Figure 10.19(b). Collector bias, on the other hand, begins to increase immediately after gate bias becomes lower than threshold voltage (Figure 10.19[c]).

To quench the injection of holes, controlled vanadium doping during 4H-SiC epitaxial growth has been demonstrated; the resultant epilayer doped with nitrogen and vanadium was reported to have a minority-carrier lifetime below 20 ns [59].

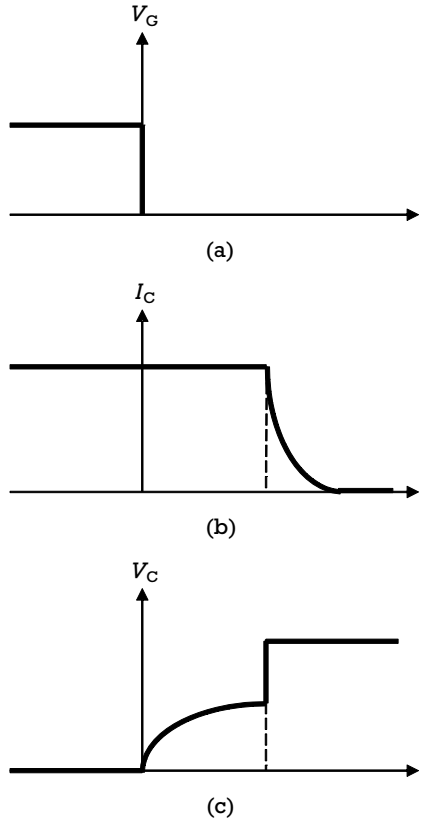

Figure 10.19 Schematic turn-off waveforms for n-channel IGBTs driving an inductive load: (a) gate bias, (b) collector current, and (c) collector bias.

10.9 Summary

This chapter first describes the optimum design of a one-dimensional structure to provide a clear understanding of GaN p-n diodes. Then, for a clear understanding of 4H-SiC p-i-n diodes, this chapter reviews stored charge and reverse recovery. With respect to power-switching devices, the chapter first discusses n-p-n BJTs from the viewpoints of collector/base design and second breakdown. Subsequently, for a clear understanding of 4H-SiC thyristors, the chapter describes Shockley diodes. Finally, the chapter provides a brief introduction to the reported blocking voltage of 4H-SiC n-channel IGBTs and their typical turn-off waveforms.

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CHAPTER

11

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11.3 SM-JTE for 4H-SiC Power Devices

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11.6 Summary

Edge Terminations

11.1 Introduction

When a SBD is unterminated, the electric field around it is enhanced at a sharp edge of the Schottky electrode (point A in Figure 11.1[a]). Although amorphization of GaN [1, 2] and SiC [3] surfaces by using argon-ion implantation successfully relieved such electric-field enhancement, suppressing large reverse leakage, which is possibly due to residual crystalline defects, is difficult. A commonly used approach for screening such an enhanced electric field in the case of silicon SBDs is to incorporate a p^+ guard ring (Figure 11.1[b]). However, in the case of GaN SBDs, magnesium-ion implantation is not an established technique (see Section 7.3.1). In the case of 4H-SiC SBDs, on the other hand, diffusion of ion-implanted aluminum is negligible (see Section 7.4). As a result, significant crowding of electric field occurs at the outer edge of the guard ring (point B in Figure 11.1[b]). Similarly, when an aluminum-ion-implanted 4H-SiC planar p-n junction is unterminated, the electric field is enhanced at the

outer edge of the p-n junction (point C in Figure 11.1[c]). Consequently, edge termination, other than that formed by amorphization and a p^+ guard ring, is indispensable for producing GaN and 4H-SiC power devices with breakdown voltage *BV* close to the ideal value.

As for an edge-termination structure of GaN power devices, a field plate (FP) [4] (Figure 11.2[a]), especially a mesa field plate (MFP) without p^+ guard rings [5] (Figure 11.2 [b, c]) or a MFP with a p^+ guard ring [6] (Figure 11.3), is frequently used. With respect to edge-termination structures formed by ion implantation, on the other hand, field-limiting rings (FLRs) (Figure 11.4[a]) [7] have the advantage that they can be incorporated with a p^+ implantation processing step. At high voltage, however, FLRs are less attractive because the spacing of each ring is limited by the capabilities of the lithography used to form it. A structure called junction termination extension (JTE) (Figure 11.4[b]) [8] is thus more favorable for fabricating high-voltage 4H-SiC power devices [9].

The biggest issue concerning JTE is its high sensitivity to the activation ratio of sheet acceptor concentration to aluminum-ion implantation dose ϕ. To relieve a sensitivity against variation of ϕ, variation of lateral doping (VLD) (Figure 11.4[c]) has been applied to silicon power devices [10]. A

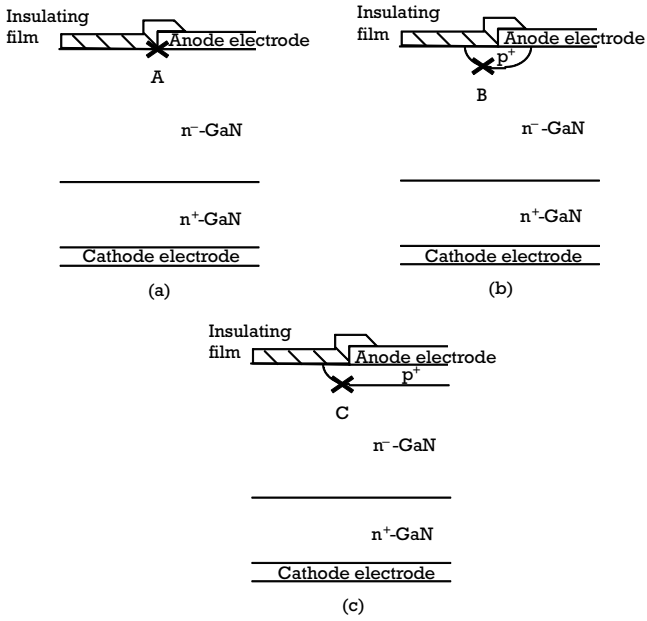

Figure 11.1 Schematic cross-sections of (a) an unterminated SBD, (b) a guard-ring-terminated SBD, and (c) an unterminated ion-implanted p^+n planar junction.

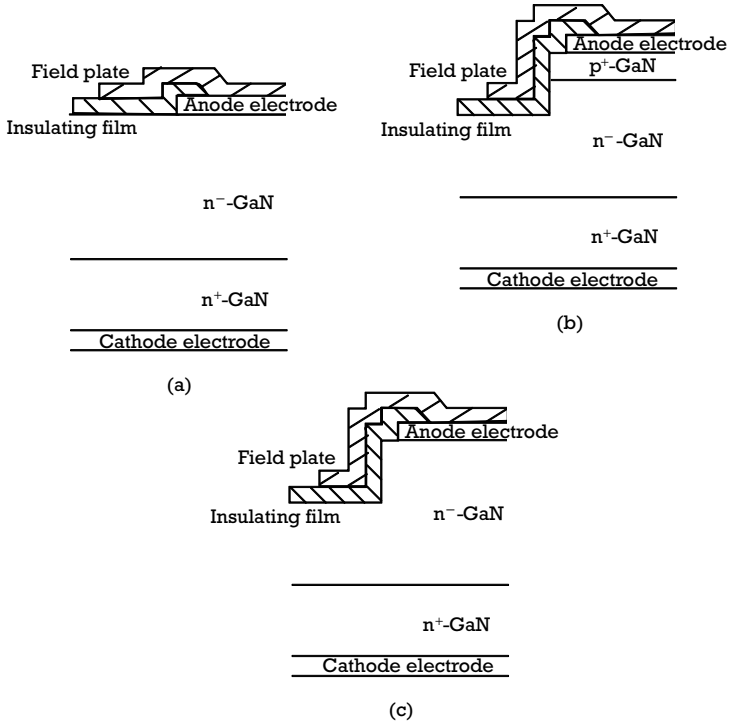

Figure 11.2 Schematic cross-sections of (a) a planar field-plate-terminated GaN SBD, (b) a mesa-field-plate-terminated GaN p-n diode, and (c) a mesa-field-plate-terminated GaN SBD.

VLD structure is fabricated in such a way that p-type dopant ions are implanted through a striped mask whose share of open areas decreases from the p^+ anode region to the edge region. The subsequent p^+ drive-in diffusion process results in a profile with decreasing doping concentration and decreasing depth toward the edge region. In the case of 4H-SiC power devices, on the other hand, drive-in diffusion is impractical due to negligible diffusivity of aluminum and anomalous diffusion of boron (see Section 7.4). Instead, several advanced types of JTEs—including the following ones that minimize the number of lithography and implantation steps—have been proposed: space-modulated JTE (SM-JTE) (Figure 11.4[d]) [11], counter-doped JTE (CD-JTE) (Figure 11.4[e]) [12], and hybrid-JTE (Figure 11.4[h]) [13], which combines ring-assisted JTE (RA-JTE) (Figure 11.4[f]) and multiple-floating-zone JTE (MFZ-JTE) (Figure 11.4[g]). It should be noted that surface of 4H-SiC is usually passivated with SiO_2, and the positive charge at the SiO_2/4H-SiC interface (Q_f) compensates the negatively ionized acceptors in the JTE region [14–16]. A JTE that has a greater tolerance to ϕ can thus have a greater tolerance to Q_f [12].

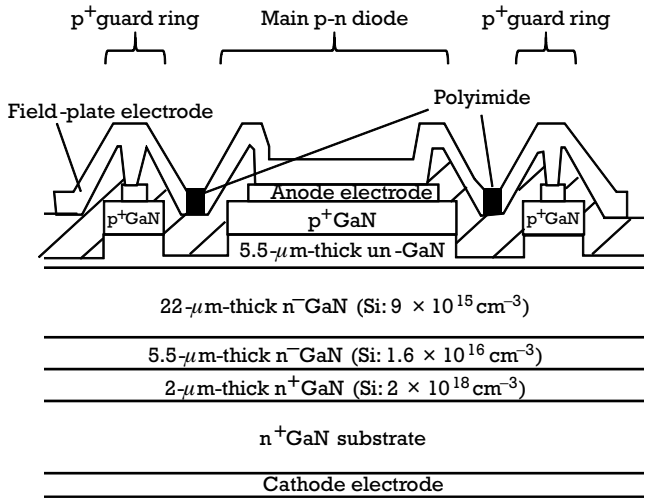

Figure 11.3 Schematic cross-section of a guard-ring-assisted mesa-field-plate-terminated GaN p-n diode [6].

Conventional FP, FLR, and JTE terminations are described in detail in some textbooks [17, 18]. Namely, in the case of FP, the influences of field-insulator thickness and FP length on *BV* of 4H-SiC Schottky and p-n junctions have been numerically calculated [18]. With respect to *BV* of a p-n junction terminated with FLR, an analytical expression is given in the case of a single field-limiting ring [18], while numerically calculated results are exemplified in the case of a 4H-SiC p-n junction terminated with multiple field-limiting rings [17]. As for JTE, numerically calculated *BV* of a 4H-SiC p-n junction is shown as a function of sheet acceptor concentration in single- [18] and two-zone [17] JTE. Therefore, this chapter describes only MFPs for GaN power devices and SM-, CD-, and hybrid-JTE for 4H-SiC power devices.

11.2 MFP for GaN Power Devices

11.2.1 MFP Without Guard Rings

In a GaN p-n diode terminated with an MFP without guard rings (Figure 11.2[b]), the field-plate electrode covers the edge of the anode electrode over the insulating layer, which spreads the depletion region in the n^--type GaN layer along the mesa surface. After such an MFP was first applied to GaN p-n diodes in 2011 [5], MFP-terminated GaN MISFETs [19] and MFP-terminated GaN SBDs [20] (Figure 11.2[c]) were reported in 2014 and 2015, respectively. The MFP edge terminations used in these devices were

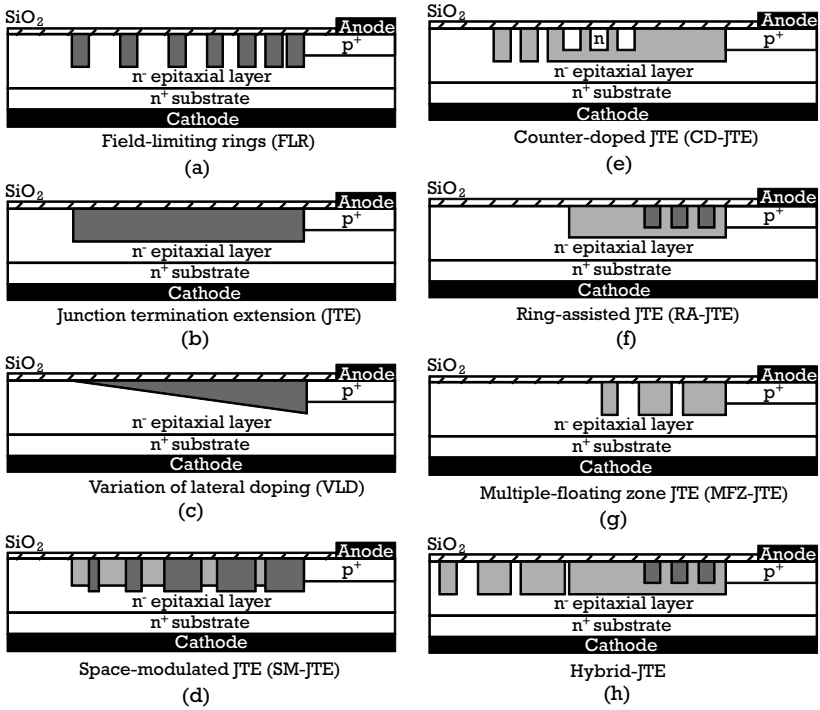

Figure 11.4 Schematic cross-sections of (a) FLRs, (b) a JTE, (c) a variation of lateral doping (VLD), (d) a space-modulated JTE (SM-JTE), (e) a counter-doped JTE (CD-JTE), (f) a ring-assisted JTE (RA-JTE), (g) a multiple-floating-zone JTE (MFZ-JTE), and (h) a hybrid-JTE.

formed on SiO_2/spin-on-glass (SOG) insulating layers [5] or on SiO_2/Al_2O_3 insulating layers [19, 20].

In 2012, 4H-SiC power devices with high-k dielectric FP terminations were studied by simulation [21]. According to the results of that study, a high-k film generates a wider depletion region than that using a SiO_2 film with the same thickness. In the simulation, Si_3N_4 and HfO_2 were used as insulating layers in a planar FP (as shown in Figure 11.2[a]). In 2016, a 0.7-μm-thick mixed oxide film consisting of CeO_2:SiO_2 at a ratio of 2:1 was applied as an MFP for GaN p-n diodes [22]. Although relative permittivity k of CeO_2 is 26, k of the mixed oxide was lowered to 12.3 [22], which is much closer to that of GaN (i.e., 10.4 [23]) compared to that of SiO_2 (i.e., 3.9). This structure led to more uniform reverse-current flow and avalanche breakdown-immune characteristics. Shown as solid circles in Figure 11.5, GaN p-n diodes terminated with an MFP using the mixed oxide (CeO_2:SiO_2) showed stable breakdown at 2.2 kV. In contrast, GaN diodes terminated with an MFP using SiO_2 suddenly broke at 2.2 kV (open circles in Figure 11.5).

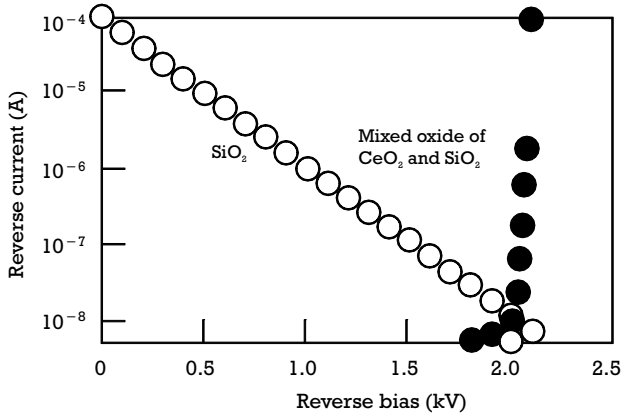

Figure 11.5 Reported reverse-current/voltage characteristics of GaN p-n diodes terminated with a MFP using SiO_2 (open circles) and mixed oxide of CeO_2 and SiO_2 (solid circles) [22].

11.2.2 Guard-Ring-Assisted MFP

A cross-section of a GaN p-n diode terminated with a guard-ring-assisted MFP is schematically shown in Figure 11.3 [6]. A p^+ guard ring is formed around the main p-n diode, and a polyimide resistor is inserted between the guard ring and the p-n diode. Without such a resistor, a p-n diode could be damaged at the outermost ring when a reverse bias is applied to it. The resistor creates a voltage drop between the p-n diode and the guard ring, thereby increasing *BV* from 4.8 to 5.0 kV [6].

11.3 SM-JTE for 4H-SiC Power Devices

In the case of SM-JTE, multiple rings with modulated width and spacing are embedded in a uniformly doped JTE region. Simulated breakdown voltage of 600-μm-wide SM-JTE applied to 4H-SiC p-i-n diodes (with 150-μm-thick i-layer doped at 1×10^{14} cm^{-3}) is shown in Figure 11.6 [24]. The aluminum doses for the rings and JTE region are respectively 1.8×10^{13} and 4.5×10^{12} cm^{-2}. It is clear from Figure 11.6 that compared to uniformly doped JTE, SM-JTE offers a much wider optimum window of JTE dose to obtain nearly ideal *BV*.

11.4 CD-JTE for 4H-SiC Power Devices

In the case of CD-JTE, n-type counter-doping is used to create the effect of multiple zones in a uniformly p-type-doped JTE region [12]. As shown by

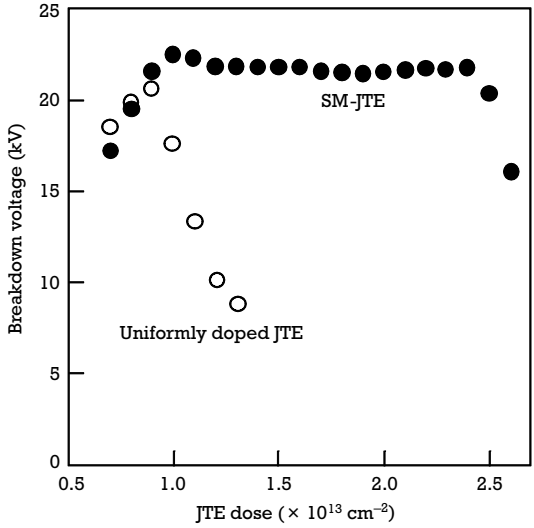

Figure 11.6 Reported dependences of simulated breakdown voltage of 4H-SiC p-i-n diodes (with 600-μm-wide JTEs) on JTE dose. Thickness and donor concentration of the i-layer are respectively 150 μm and 1×10^{14} cm^{-3}. As for SM-JTE, an optimum dose window for obtaining nearly ideal breakdown voltage is remarkably enlarged [24]. SM-JTE has been applied to 21-kV 4H-SiC p-i-n diodes [25] and 21-kV 4H-SiC BJTs [26].

the open circles in Figure 11.7, *BV* of 4H-SiC p-i-n diodes terminated with uniformly doped JTE degrades when Q_f is positive. In contrast, *BV* of p-i-n diodes terminated with CD-JTE degrades little up to $Q_f = 6 \times 10^{12}$ cm^{-2} (solid circles in Figure 11.7), and that lack of *BV* degradation indicates superior robustness of *BV* against process variation [12].

11.5 Hybrid-JTE for 4H-SiC Power Devices

While floating rings are inserted in a uniformly doped region in a RA-JTE (Figure 11.4[f]) [9, 27], dose is gradually distributed in the manner of VLD in a MFZ-JTE (Figure 11.4[g]) by controlling the width of the discrete implanted regions (i.e., zones) [28]. RA-JTE and MFZ-JTE were first optimized by Sung and Baliga. With respect to 4H-SiC p-i-n diodes with a 40-μm-thick, 2×10^{15}-cm^{-3}-doped drift layer, the optimized widths of the former and latter JTE were respectively 120 and 90 μm [29]. Six 3-μm-wide p^+ rings, with spacing varied from 3 to 8 μm, were used in the optimized RA-JTE, while the width of i-th zone W_i (i = 2, 3, … 10) was varied as 10 (μm)/(1.07 × [i −1]). A hybrid-JTE was then constructed by narrowing the width of the optimized RA-JTE to 90 μm and placing the narrowed RA-JTE near the p^+ main junction and the 90-μm-wide MFZ-JTE next to the

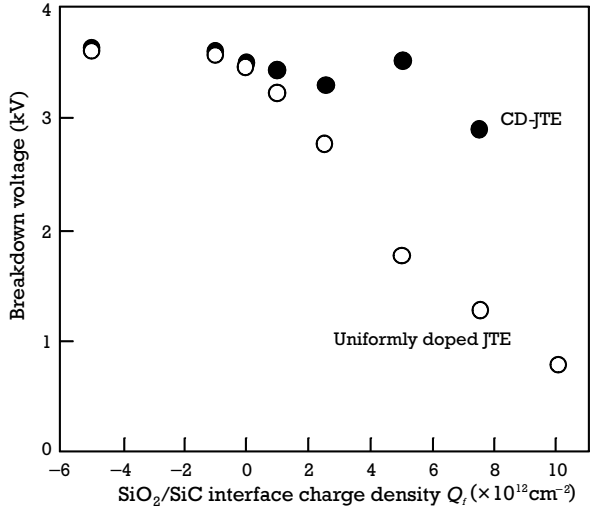

Figure 11.7 Reported dependences of simulated breakdown voltage of 4H-SiC p-i-n diodes with a 100-μm-wide CD-JTE (solid circles) and a uniformly doped JTE (open circles) on SiO_2/SiC interface-charge density. Thickness and donor concentration of the i-layer are respectively 30 μm and 2×10^{15} cm^{-3} [12].

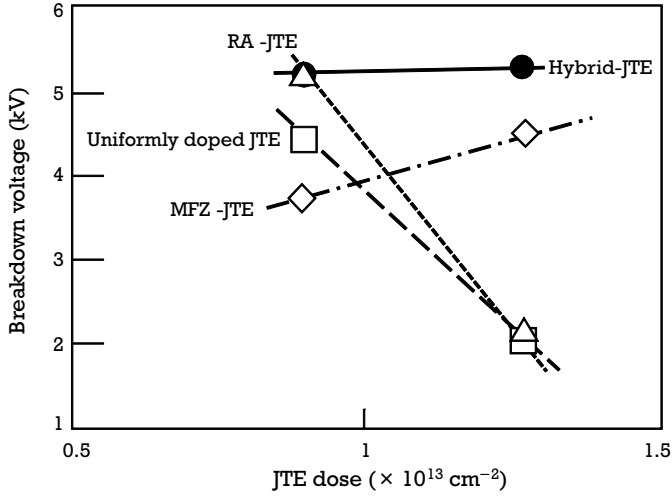

Figure 11.8 Reported JTE dose dependence of measured breakdown voltages of 4H-SiC p-i-n diodes with 180-μm-wide hybrid-JTE, 120-μm-wide RA-JTE, 90-μm-wide MFZ-JTE, and 120-μm-wide uniformly doped JTE. Thickness and donor concentration of the i-layer are, respectively, 40 μm and 2×10^{15} cm^{-3}. The JTE doses of 9×10^{12} and 1.25×10^{13} cm^{-2} are respectively estimated from the implanted doses of 1.3×10^{13} and 1.8×10^{13} cm^{-2} under the assumption of activation ratio of 70% [29].

RA-JTE (Figure 11.3[h]). As shown in Figure 11.8, a high dose in the optimized RA-JTE and uniformly doped JTE drastically reduce *BV*. This reduction was attributed to a high electric field at the outer edge of the JTEs [29]. Since the dose dependence of *BV* of the optimized MFZ-JTE is opposite to that of the optimized RA-JTE and that of the uniformly doped JTE, as for the hybrid-JTE, the optimum dose window for obtaining nearly ideal breakdown voltage is enlarged.

11.6 Summary

This chapter introduces mesa-field-plate termination structures for GaN power devices, as well as space-modulated-, counter-doped-, and hybrid-JTEs for 4H-SiC power devices as advanced termination structures. Readers should also refer to the latest papers on termination structures for vertical GaN and 4H-SiC power devices , since related research is still being actively conducted.

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CHAPTER

12

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12.3 Tolerance to HTGB Stress

12.4 Tolerance to H3TRB Stress

12.5 Tolerance to TC Stress

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12.7 Tolerance to Terrestrial Cosmic Radiation

12.8 Summary

Reliability of Vertical GaN and SiC Power Devices

12.1 Introduction

This chapter describes reported reliability tests on vertical GaN and 4H-SiC power devices. They are based on JEDEC [1] and JEITA [2] standards for silicon power devices and cover high-temperature reverse bias (HTRB), high-temperature gate bias (HTGB), high-humidity, high-temperature reverse bias (H3TRB), thermal cycling (TC), and high-temperature operating (HTO), and terrestrial cosmic radiation.

12.2 Tolerance to HTRB Stress

HTRB tests verify long-term stability of semiconductor-chip leakage. Semiconductor chips or power modules (Figure 12.1) are stressed with a reverse voltage (e.g., 80% of the rated blocking capability of power devices) at an ambient temperature of their operational limit.

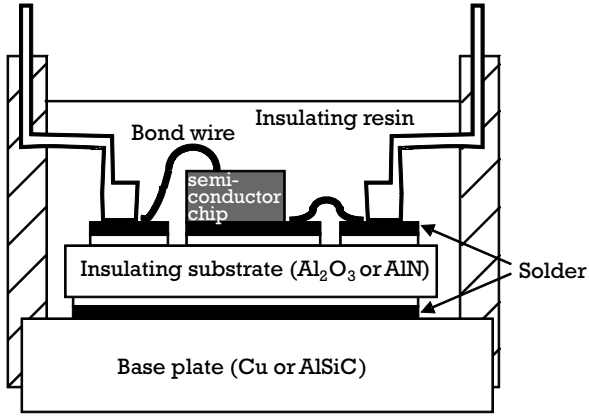

Figure 12.1 Schematic cross-section of a typical power module.

Mobile ions, possibly contaminations during assembly or residue of solder flux, can accumulate in high electric-field areas and generate a surface charge. The surface charge can alter the electric field in power devices and generate additional leakage [3].

In the case of vertical GaN power devices, substrate orientation has been reported to play a significant role in tolerance to HTRB stress. While on-axis epitaxial growth of GaN results in large hexagonal hillocks due to spiral growth around a screw dislocation (see Section 6.2), introducing a slight miscut of several tenths of a degree makes step-flow growth (see Section 6.5) overwhelm spiral growth. Use of step-flow growth resulted in 231 (i.e., 77/lot × 3 lots) GaN p-n diodes (rated at 1,200V and 10A) passing 1,000-h HTRB tests at 960V and 150°C. Moreover, threshold voltage V_{th}, specific on-resistance $R_{on}A$, and forward drain current of GaN normally-on-junction field-effect transistors did not shift before and after 788-h HTRB tests [4]. With respect to normally-off transistors, over-300-h stability of V_{th} and off-state leakage I_{DS} (at drain-source bias V_{DS} = 400V) of 1.7-kV GaN p^+-gate heterojunction field-effect transistors was reported [5], as described in Section 9.5.3 (Figure 12.2).

In the case of MISFETs (see Section 9.7), an HTRB test stresses not only the p-n junction at the drain but also the gate insulator. According to the results of tests on commercial-off-the-shelf 4H-SiC MISFETs (rated at 1,200V and 42A) [6], after 378-h HTRB stress of 960V at 150°C, a drain-source short occurred in one of four 4H-SiC MISFETs. As shown in Figure 12.3, the other three MISFETs showed drain leakage at different levels as stress time increased. Possible mechanisms of such drain-leakage degradation include drain-to-source subthreshold leakage, band-to-band-tunneling-dominated p-n junction leakage, and interface-trap-induced leakage [6].

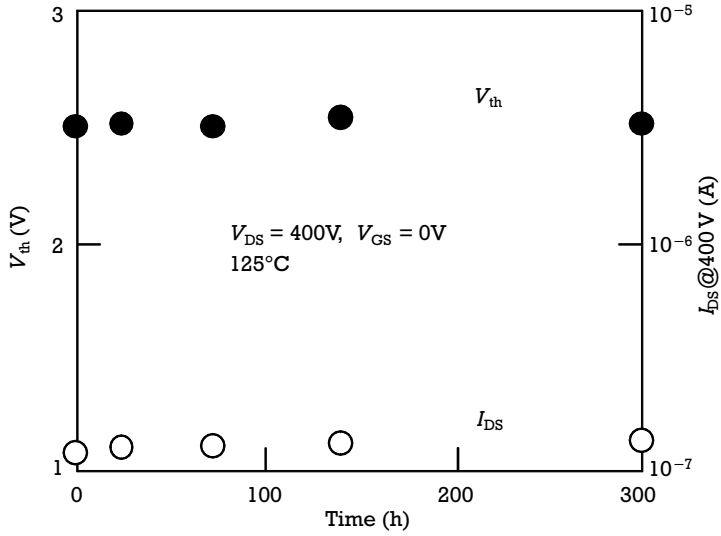

Figure 12.2 Reported results of HTRB tests on vertical GaN transistors on GaN substrates [5].

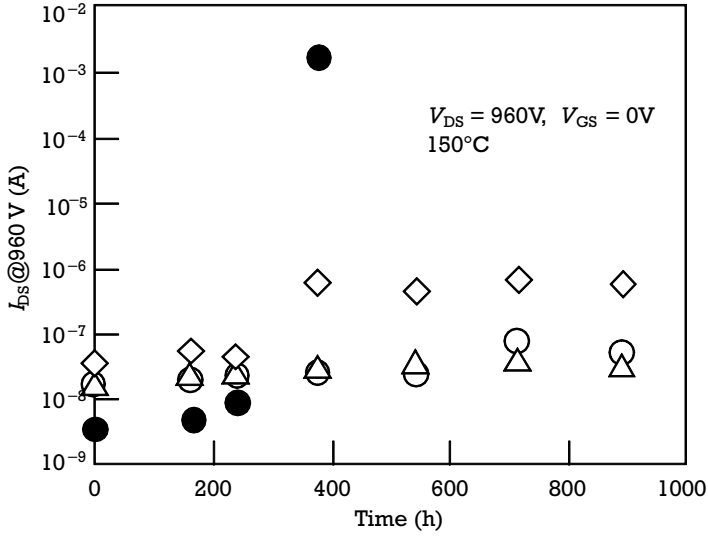

Figure 12.3 Reported results on HTRB tests of commercial-off-the-shelf 4H-SiC MISFETs [6].

Moreover, in an HTRB test at 152°C and 90% of the rated voltage of commercial 1.2–1.7-kV 4H-SiC MISFET power modules (rated at 120–400A) [7], three out of five modules did not pass the test, showing

that the tolerance of 4H-SiC MISFET modules to HTRB stress needs to be further improved.

12.3 Tolerance to HTGB Stress

In HTGB tests, variation in V_{th} is monitored after prolonged gate-source bias V_{GS} is applied to MISFETs at high temperature. Commercial-off-the-shelf 4H-SiC MISFETs (rated at 1,200V and 42A) have been tested at 150°C [6]. As shown by solid and open symbols in Figure 12.4, positive and negative V_{GS} stresses respectively cause positive and negative shifts in V_{th}. This effect is attributable to electrons tunneling into or out of insulator traps in response to the electric field produced by V_{GS} stress [8, 9].

12.4 Tolerance to H3TRB Stress

In H3TRB tests, penetration of moisture through an insulating resin (Figure 12.1) is accelerated under high humidity, high temperature, and high reverse bias to verify the reliability of power modules. In the case of silicon IGBT power modules, corrosion has been reported to build up due to the formation of a closed water film linking the chip metallization of the active area being the negative electrode [10]. According to a first report on

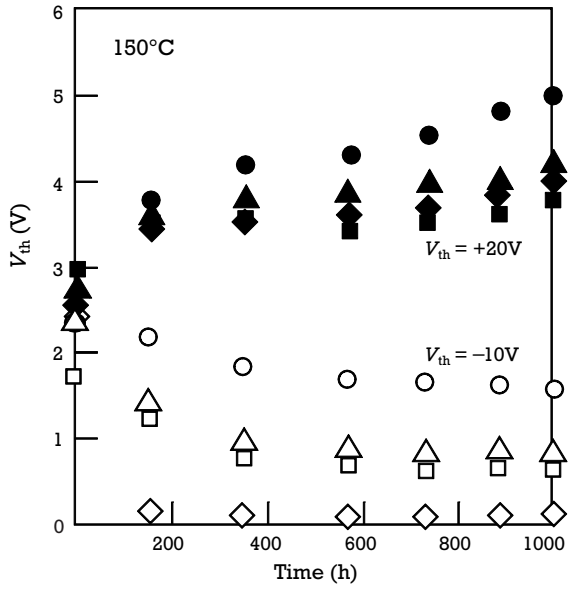

Figure 12.4 Reported results of HTGB tests on commercial-off-the-shelf 4H-SiC MISFETs. (Solid symbols: V_{GS} = + 20V and 150°C; open symbols: V_{GS} = –10V and 150°C [6].)

H3TRB tests (at 85°C, 85% relative humidity, and 80V) of GaN p-n diodes, a few diodes failed after 850 hours due to delamination caused by water ingress from chip edges. After improving the encapsulation dielectric layer, however, no diodes failed in further H3TRB tests [4].

According to the reported results of H3TRB tests on commercial 0.3–0.8-kV 4H-SiC MISFET power modules at 90°C, 90% relative humidity, and 65% rated voltage, two out of five modules failed after 690 and 860 hours; the former was due to failure of the diode connected with the MISFET chip, and the latter was due to failure in the gate oxide [7]. It should be noted that even in the case of three modules that passed the H3TRB test, $R_{on}A$ increased, showing that tolerance of 4H-SiC MISFET power modules to H3TRB stress needs to be further improved.

12.5 Tolerance to TC Stress

A TC test induces an accelerated thermomechanical stress on power modules that consists of several materials with different thermal-expansion coefficients. In the case of silicon IGBT power modules, the most dominant failure is bond-wire liftoff [11]. It was reported that 385 (i.e., 77/lot × 5 lots) GaN p-n diodes (rated at 1,200V and 10A) passed 1,000-cycle TC tests when temperature was varied from −65°C to 150°C [4]. It was also reported that five TC-tested 4H-SiC MISFET commercial power modules passed 1,186 cycles when temperature varied was from −50°C to 150°C [7].

12.6 Tolerance to HTO Stress

When an excited minority carrier recombines with an electronic center associated with a defect, the recombination energy is known to be released nonradiatively to induce local vibrations of the defect, which leads to some rearrangement of the defect itself [12, 13]. Although GaN-based devices have high dislocation density, their lifetimes have been reported to be long due to large shear stress under dislocation motion [14]. An HTO test on 77 GaN p-n diodes under forward current density of 20 kA/cm^2 at junction temperature of 275°C actually showed no degradation of the current/voltage characteristics [4].

In contrast, electron-hole recombination at a BPD (see Section 2.2.3) in the drift layer of 4H-SiC bipolar devices induces nucleation and expansion of recombination-enhanced stacking faults, which increases their forward voltage V_F [13, 15]. Dislocation motion in 4H-SiC seems to be caused by lowering the energy of the material system (see Section 2.2.3), not by applying shear stress [15]. Such recombination-induced stacking faults also degrade performance of 4H-SiC unipolar devices. For example, it was reported that

when the body diode of a 4H-SiC MISFET with a 100-μm-thick, 6×10^{14} cm^{-3}-doped drift layer (Figure 12.5[a]) was forward-biased ($V_{GS} = -10V$) for one hour, V_F increased, in a similar manner to that observed in the case of 4H-SiC p-i-n diodes (Figure 12.5[b]) [16]. In another report, 4H-SiC MPS diodes (see Section 8.6.1) with different BPD densities were forward-biased, and it was observed that V_F increased as a function of injection time (Figure 12.6) [17]. The latter report shows that reducing BPD density is the most important issue in regard to improving tolerance of 4H-SiC power devices to HTO stress.

12.7 Tolerance to Terrestrial Cosmic Radiation

The Earth is constantly showered by cosmic radiation with highly energetic particles, mainly protons as well as light and heavy nuclei [18]. These particles collide with air molecules to give rise to cascades of secondary particles reaching the ground. Although this terrestrial cosmic radiation is made up of neutrons, protons, pions, muons, electrons, and electromagnetic waves, neutrons account for 95% of it at sea level [19]. In the case of silicon power devices, neutrons have been shown to cause failures via interactions with lattice atoms. Resultant recoiled atoms or spallation products create charge spikes along their trajectories. Because electrons are attracted to drain or collector electrodes and holes to source or gate electrodes, these attendant electrons and holes can lead to current transients, which can turn on a parasitic bipolar transistor and result in a burn-out failure. Since the hole pile-up under the gate can increase the electric field around the gate insu-

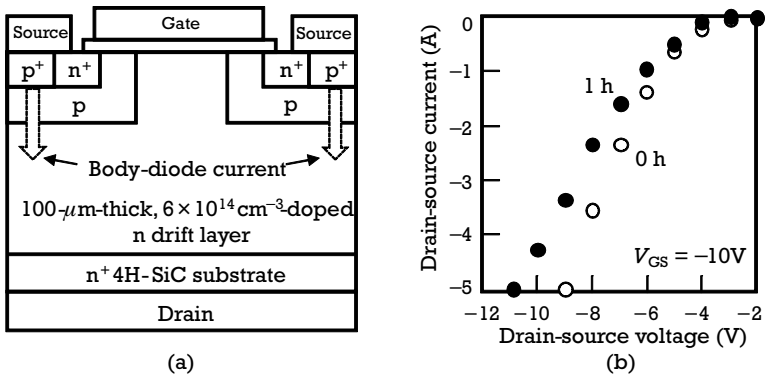

Figure 12.5 (a) Schematic cross-section and (b) reported current/voltage characteristics of a body diode in a 4H-SiC MISFET [16].

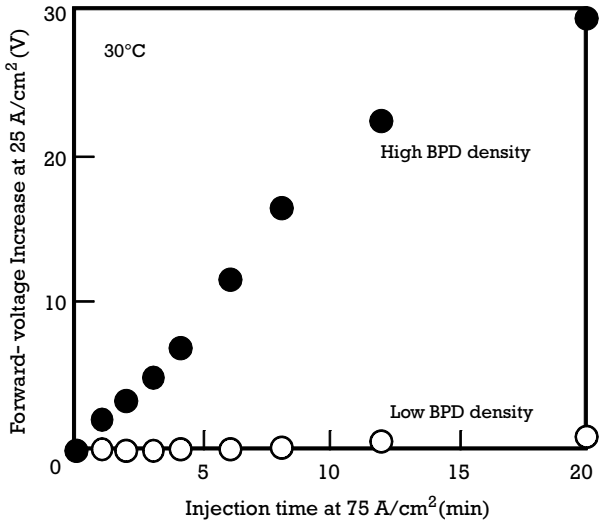

Figure 12.6 Reported forward-voltage increase in 4H-SiC MPS diodes as a function of injection time [17].

lator to the point of causing catastrophic failure, a gate rupture failure can also occur [20].

However, neutron-induced failures are not well understood in the cases of GaN and 4H-SiC power devices [20–26]. For example, in one study, GaN p-n diodes were exposed to 1-MeV 3×10^{13}-cm^{-2} neutrons [21]. According to the results of that study, $R_{on}A$ increased from 2–3 mΩcm^2 by 3 mΩcm^2, while breakdown voltage BV decreased from 1,740V by 80V. Such degradation of $R_{on}A$ and BV indicates that both on- and off-state performances are impacted by radiation-induced defects within the drift region of GaN p-n diodes. On the other hand, when tolerances of commercial silicon and 4H-SiC MISFETs to terrestrial neutron radiation were compared [20], it was found that although neutrons give rise to fewer failures in SiC MISFETs compared to silicon MISFETs, the failure modes in SiC MISFETs can differ depending on the vendor. These results show that tolerances of vertical GaN and 4H-SiC power devices to terrestrial cosmic radiation have to be further investigated.

12.8 Summary

This chapter briefly describes reported results of HTRB-, HTGB-, H3TRB-, TC-, HTO-, and terrestrial cosmic radiation tests on vertical GaN and 4H-SiC power devices. Readers should refer also to the latest papers on such reliability tests because related research is still being actively conducted.

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